STLED325

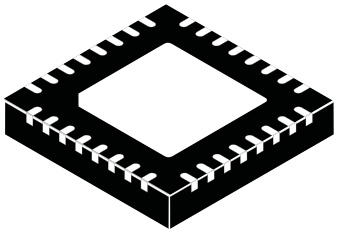
I²C interfaced, advanced LED controller/driver with keyscan, standby power management and real time clock (RTC)

Features

- LED controller driver with 13 outputs (8 segments/5 digits)
- Standby power management to host
- Integrated low-power, accurate RTC
- Integrated remote control decoding:
  - Philips (RC5, RCMM)
  - Thomson (RCA, R2000)
  - NEC and R-STEP
- Wake-up using front panel keys, remote control, real time clock (RTC), extra pin (AV or CEC)
- Battery or super-cap back up mode for real time clock (RTC)
- Keyscanning (8x2 matrix)
- Low power consumption in standby mode
- I^2C serial bus interface (SCL, SDA)
- 16-step dimming circuit to control the display brightness
- 5.0 V (± 10%) for V_{CC}
- Built-in thermal protection circuit
- External crystal with internal oscillator for real time clock (RTC)

Applications

- Set-top boxes
- White goods
- Home appliances
- DVD players, VCRs, DVD-R



QFN32
(5 x 5 mm)

Description

The STLED325 is a compact LED controller/driver that interfaces microprocessors to LED displays through serial I^2C interface. It drives LEDs connected in common anode configuration and includes keyscanning for an 8 x 2 key matrix which automatically scans and de-bounces a matrix of up to 16 switches.

Furthermore, the STLED325 provides standby power management to the host. It also integrates a low-power, highly-accurate RTC and a remote-control decoder. All functions are programmable using the I^2C bus. Low power consumption during standby mode is achieved.

The STLED325 controller/driver is ideal as a single peripheral device to interface the front panel display with a single-chip host IC like CPU.

Table 1. Device summary

Order code	Temp range (°C)	Package	Comments
STLED325QTR	-40 to +85 °C	QFN32	250 parts per reel

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1 Description

The STLED325 is a compact LED controller/driver that interfaces microprocessors to LED displays through serial I^2C interface. It drives LED connected in common anode configuration. The STLED325 drives up to 40 discrete LEDs in 8 segment/5 digit configuration while functioning from a supply voltage of 5 V. The maximum segment current for the display digits is set through a single external resistor. Individual digits may be addressed and updated without rewriting the entire display. Additionally it includes keyscanning for an 8 x 2 key matrix which automatically scans and de-bounces a matrix of up to 16 switches.

Furthermore, it provides standby power management to the host. The STLED325 also integrates a low-power, highly-accurate RTC and a remote-control decoder. All functions are pro-grammable using the I^2C bus. Low power consumption during standby mode is achieved. STLED325 supports numeric-type displays and reduces the overall BOM costs through high integration. Also it provides ESD protection of greater than 2 kV HBM.
The LED controller/driver is ideal as a single peripheral device to interface the front panel display with a single-chip Host IC like CPU.

2 Functional and application diagram

Figure 1. Functional block diagram

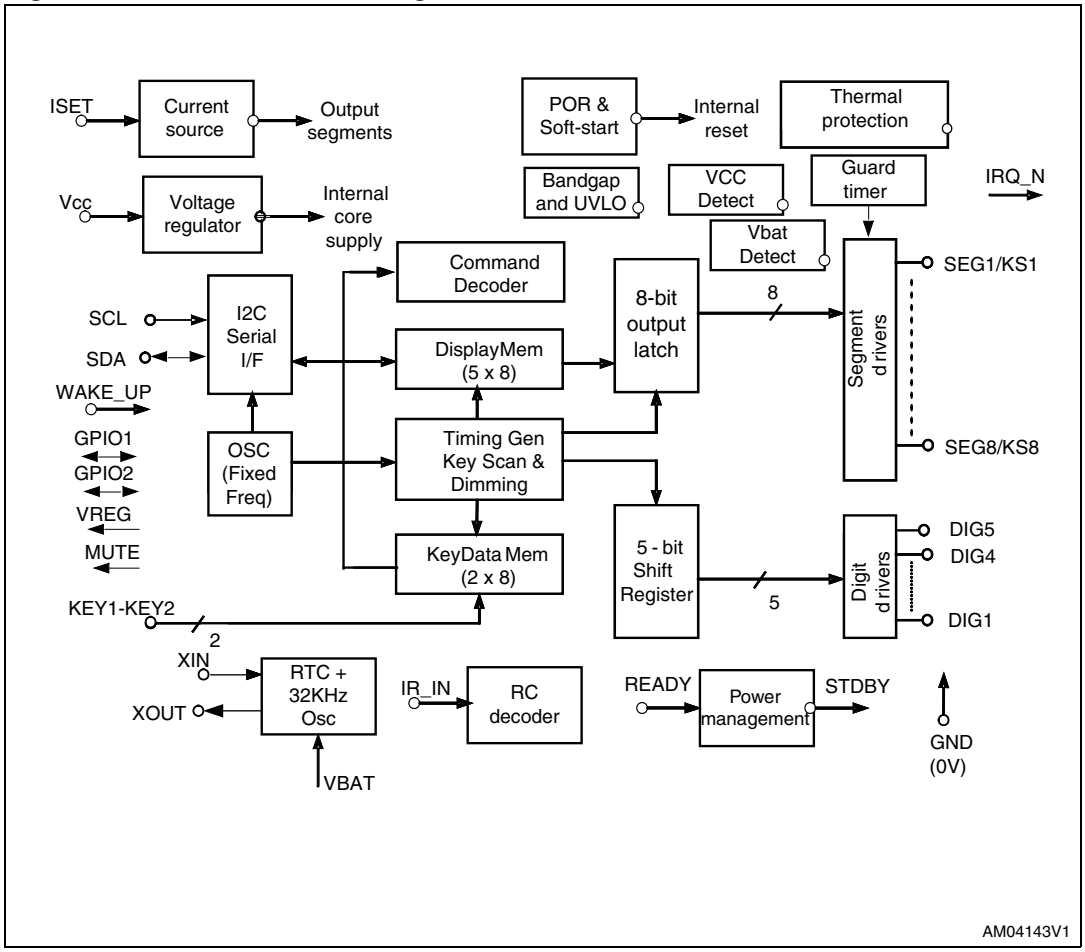


Figure 2. Application diagram

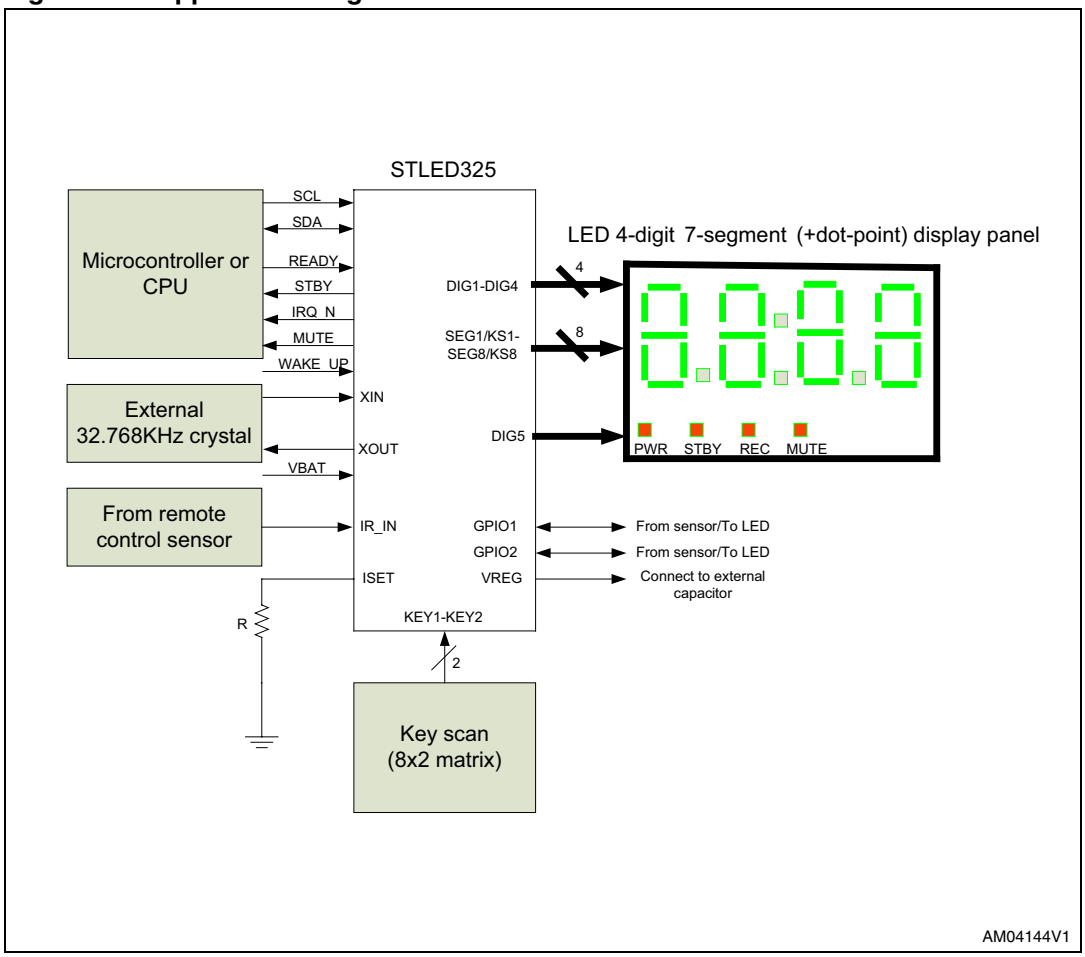
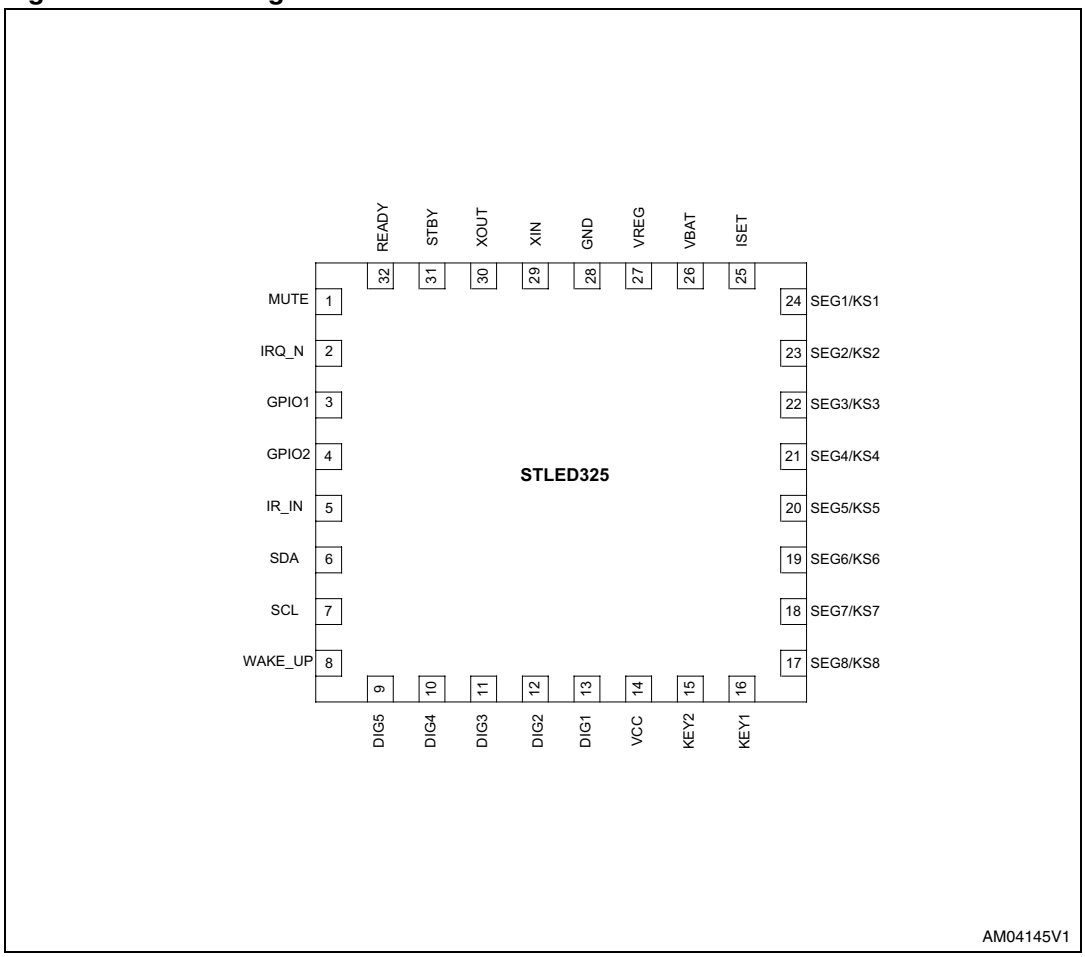


Figure 3. Pin configurations



3 Functional description

The STLED325 is a common anode LED driver controller which can be used to drive red, green or blue LEDs as the current is adjustable through the external resistor. In the common anode configuration, the digit outputs source the current to the anodes while the segment outputs sink the current from the cathodes. The configurable output current can be used to drive LEDs with different current ratings (red, green or blue). The brightness can be controlled through the I^2C interface as described later. The outputs can be connected together in parallel to drive a single LED. In this case, two parallel current sources of equal value drive a single LED. The external resistor value can be set accordingly to determine the desired output current.
Soft-start limits the inrush current during power-up. The built-in thermal protection turns off the display when the temperature exceeds 140°C with a small hysteresis of 15°C. The display is blanked (LEDs are turned off or in high-Z state) on power-up.

3.1 Low power mode of operation

When not used, the STLED325 goes into low power mode of operation wherein the current consumption drops to less than 1 mA. During this mode, the data configured is maintained as long as the supply voltage is still present (the contents of the internal RAM need the supply voltage to be present). Port configuration and output levels are restored when the STLED325 is taken out of shutdown. For minimum supply current in shutdown mode, logic inputs should be at GND or V_{CC}.

3.2 I^2C serial interface

The interface is used to write configuration and display data to the STLED325. The serial interface comprises of a shift register into which SDA is clocked on the rising edge of the SCL after a valid start of communication. When communication is stopped, transitions on SCL do not clock in the data. During this time, the data are parallel-loaded into a latch. The 8-bit data is then decoded to determine and execute the command.
For an overflow condition, if more bytes are written, then they are ignored whereas if more bytes are read, then the extra bytes are stuffed with 1's.

3.3 Initial power up

On initial power-up, all control registers are reset, the display is blanked and the STLED325 is in the low-power mode. All the outputs are in high-impedance state at initial power-up. The SDA is pulled high by an external pull-up resistor. The display driver has to be configured before the display can be used.

3.4 Display types

Figure 4. Display types

Seven segment display with dot point and common-anode LED panel

3.5 Keyscan

The full keyscan is illustrated in the later section of the datasheet. One diode is required per key switch. The keyscan circuit detects any combination of keys being pressed during each de-bounce cycle.
The keyscan matrix on the STLED325 passes command from the front panel to the host processor through the SDA pin on STLED325. The STLED325 can be programmed to wake-up the system from standby using any of the 16 keys pressed on the front panel. These wake-up keys are also referred to as hot-keys.

3.6 Timers

3.6.1 Guard timer

For safety related applications, a guard timer is integrated in the STLED325. The guard timer gives enhanced reliability to the device.

The guard timer can be used to detect an out of-control microprocessor. The user programs the guard timer by setting the desired amount of time-out into the Guard timer. This guard time has an initial de-fault value of 10s upon first power-up and subsequently can be configured from 1s to 15s during normal operation. If a time period of longer than 15s is desired, then the watchdog timer from RTC can be used. It can also be disabled after first power-up. If the processor does not clear the timer within the specified period, the STLED325 puts the system in the standby mode.

This is only active from L to H transition on READY or WAKE_UP pin but it is not level-based. The guard timer count is cleared by the guard timer clear/reset bit. While in normal mode, the count starts from the previously count value that was in the register. During the cold boot up or warm boot up, the count starts from the configured value.

3.6.2 Watchdog timer

Another watchdog timer is present in the Watchdog timer register at address 09h of the RTC register map. This watchdog timer can be used to program timer values of greater than 15s. Bits BMB4-BMB0 store a binary multiplier and the three bits RB2-RB0 select the resolution where:

000 = 1/16 second (16 Hz);

001 = 1/4 second (4 Hz);

010 = 1 second (1 Hz);

011 = 4 seconds (1/4 Hz); and

100 = 1 minute (1/60 Hz).

The Watchdog timer is programmed by setting the desired timeout into the Watchdog register, address 09h. The amount of timeout time is determined to be the multiplication of the 5-bit multiplier value with the resolution values depicted by the watchdog resolution bits.

The Watchdog timer is disabled when its register is cleared by writing a value of 00h.

Hence the Watchdog function is not enabled upon power on. It is enabled when a non-zero value is written into its register. The Watchdog timer is reset by performing a write to the watchdog register, then the time-out period starts over.

If the processor does not reset the timer within the specified timeout period, and when the timeout occurs, the watchdog flag is set. The watchdog timer of RTC is cleared by writing a 00 value and starts again whenever any new value is written to it.

The WatchDogEn Flag can be disabled or enabled by writing to the register bit and the reset of watchdog timer is done by writing to the register.

3.7 Power-on-reset and soft-start

The device integrates two internal power-on-reset circuits which initialize the digital logic upon power up. One circuit is for the V_{CC} power and the other is for the V_{BAT} power. The soft-start circuit limits the inrush current and high peak current during power-up. This is done by delaying the input circuit's response to the external applied voltage. During soft-start, the input resistance is higher which lowers the in-rush current when the supply voltage is applied.

3.8 LED drivers

The constant current capability is up to 40 mA per output segment and is set for all the outputs using a single external resistor. When acting as digit drivers, the outputs source current to the display anodes. When acting as segment drivers, the LED outputs sink current from the display common cathodes. The outputs are high impedance when not being used as digit or segment drivers.
Each port configured as a LED segment driver behaves as a digitally-controlled constant current sink. The LED drivers are suitable for both discrete LEDs and common anode (CA) numeric LED digits. When fully configured as a LED driver, the STLED325 controls up to 8 LED segments in a single digit with individual 8-step adjustment of the constant current through each LED segment. A single resistor sets the maximum segment current for all the segments, with a maximum of 40 mA per segment. The STLED325 drives any combination of discrete LEDs and common anode (CA) digits for numeric displays.
The recommended value of RSET is the minimum allowed value, since it sets the display driver to the maximum allowed segment current. RSET can be a higher value to set the segment current to a lower maximum value where desired. The user must also ensure that the maximum current specifications of the LEDs connected to the drivers are not exceeded.

3.9 Over temperature cut-off

The STLED325 contains an internal temperature sensor that turns off all outputs when the die temperature exceeds 140°C. The outputs are enabled again when the die temperature drops below 125°C. Register contents are not affected, so when a driver is over-dissipating, the external symptom will be the load LEDs cycling between on and off as the driver repeatedly overheats and cools, alternately turning the LEDs off and then back on again. This feature will protect the device from damage due to excessive power dissipation. It is important to have good thermal conduction with a proper lay-out to reduce thermal resistance.

3.10 Standby mode

By utilizing the standby function, the host processor and other ICs can be turned off to reduce power consumption. The STLED325 is able to wake-up the system when programmed hotkeys are detected to signal that the full operation of the system is required. The hotkeys can be entered to the system through the front panel keys or through the infrared (IR) remote control or the Real Time Clock (RTC) alarm or through the wake-up pin. STLED325 supports multiple remote control protocols decoding by setting the appropriate register.
The STLED325 is able to cut-off the power to the main board for standby operation for good power management. STBY will be set to high when READY signal goes from high to low, I^2C command for standby is seen or when the guard timer has finished counting down to 0, whichever occurs first.
In the normal mode of operation, the STBY is asserted only when the guard timer has finished counting down to 0. This is meant to put the system into stand-by even though standby command was not issued by the host or READY signal did not go low. This occurs as the guard timer register was not cleared before it finished counting down to 0.

3.10.1 Cold boot up

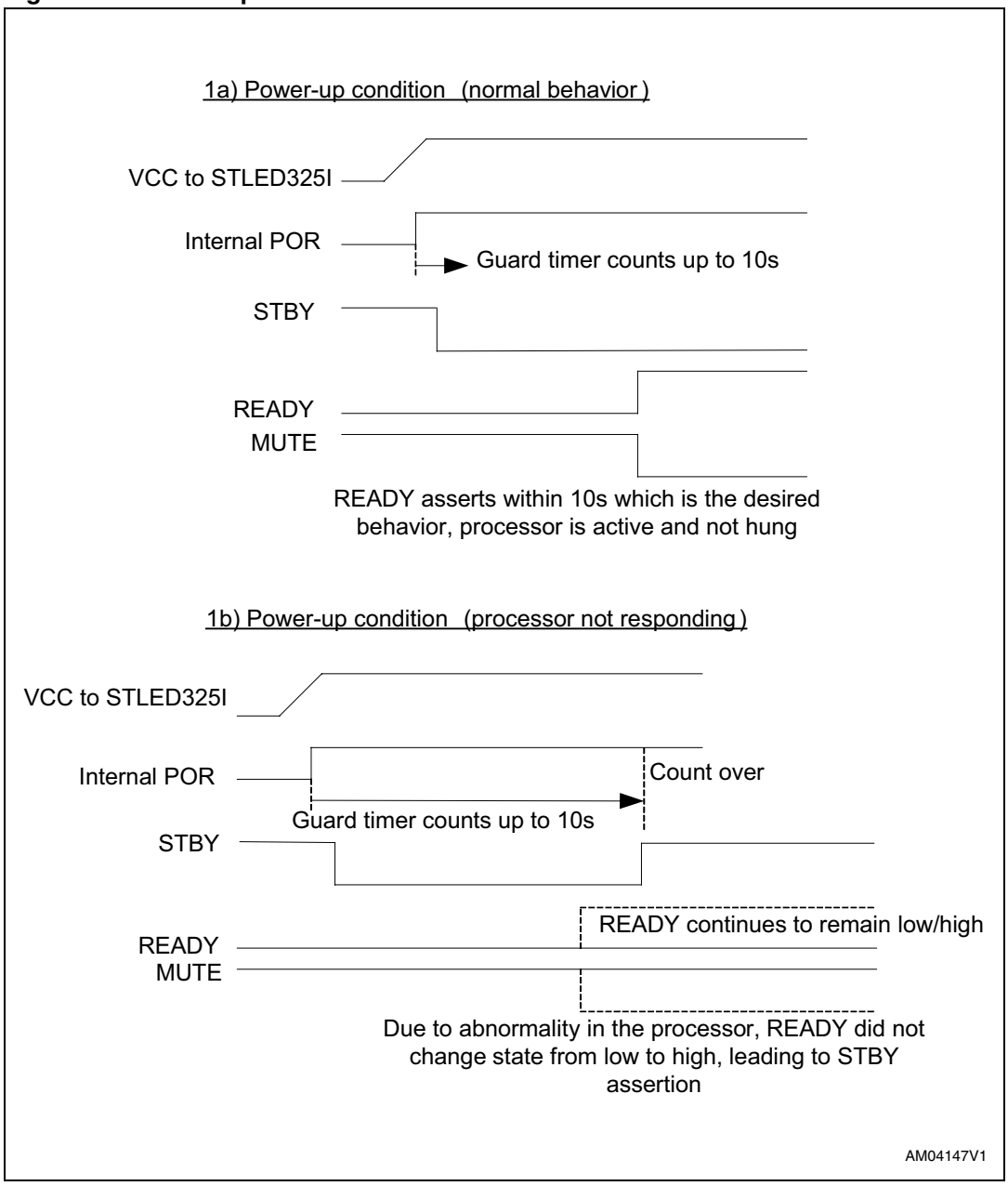
When power is first applied to the system, the STLED325 is reset. It will then manage the power to the main board by bringing the STBY pin to a low level.

This wakes up the main processor which asserts the READY pin to a high level to indicate to STLED325 of a proper boot-up sequence.

If the microprocessor does not assert the READY pin to a high within 10s (default), the STLED325 cuts off the power to the Host by asserting the STBY pin. The high level on READY pin signifies that the processor is ready. After this, the processor can configure the STLED325 by sending the various I^2C commands for configuration of display, RC protocol, RTC display mapping, hot-keys.

The power-up behavior in 2 conditions is shown in *Figure 5*.

Figure 5. Power-up condition



Note: 1 Guard timer is turned off by default upon READY assertion.

2 If Guard timer is to be kept on during READY high condition, the guard timer registers must be set accordingly by proper commands through I^2C bus.

3 In this power-up condition, Guard timer is triggered by internal POR pulse.

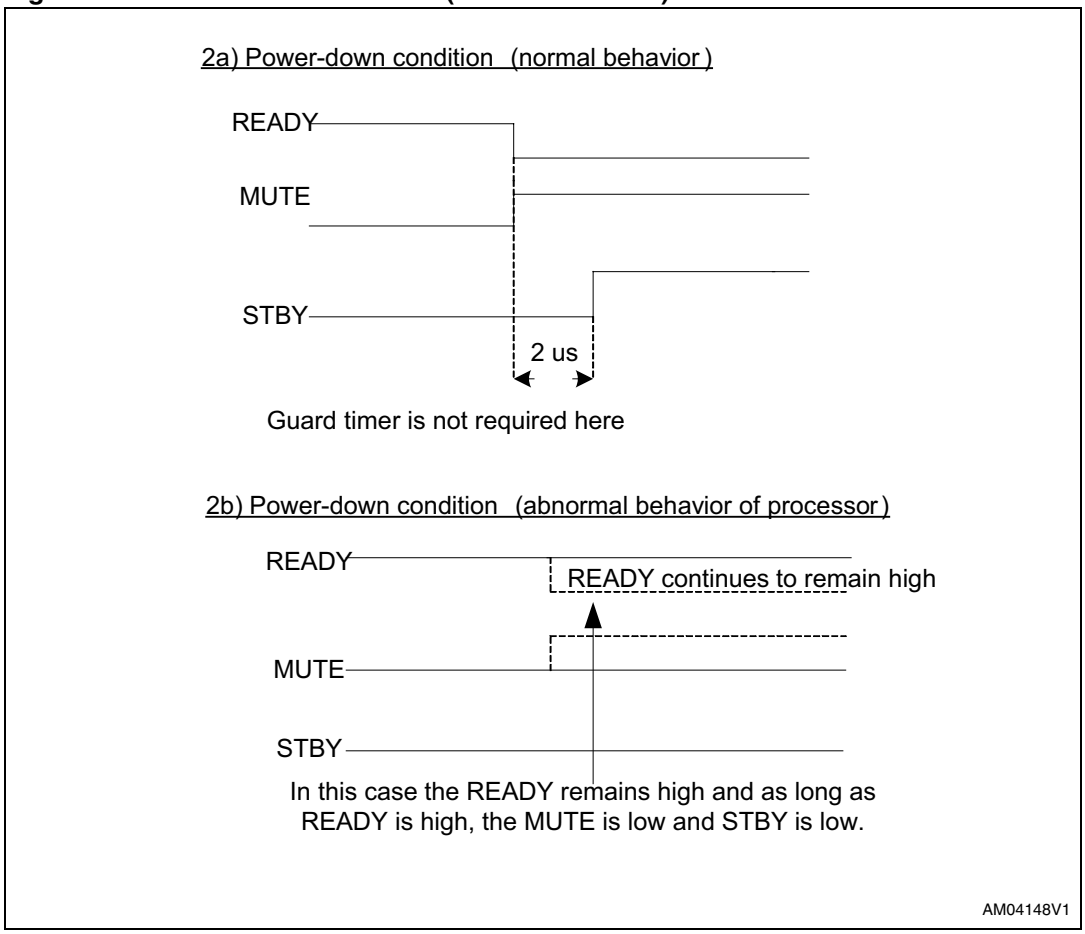
4 During power-up, the Guard timer value is 10s.

3.10.2 Entering standby mode

The STLED325 controls the power to the main board using the STBY pin. During normal operation, the STBY pin is a low level which externally controls a Power MOS switch to enable power to the main board. The STLED325 asserts the STBY pin to a high when any one of the following conditions occur:

- Processor fails to respond by enabling the READY pin within 10s upon first power-up (cold boot up)
- Guard timer counts down to 0s
- Processor makes the READY pin to low (can happen in various conditions such as user presses STBY key on front panel, STBY key on remote control, etc).

Figure 6. Power down condition (normal behavior)



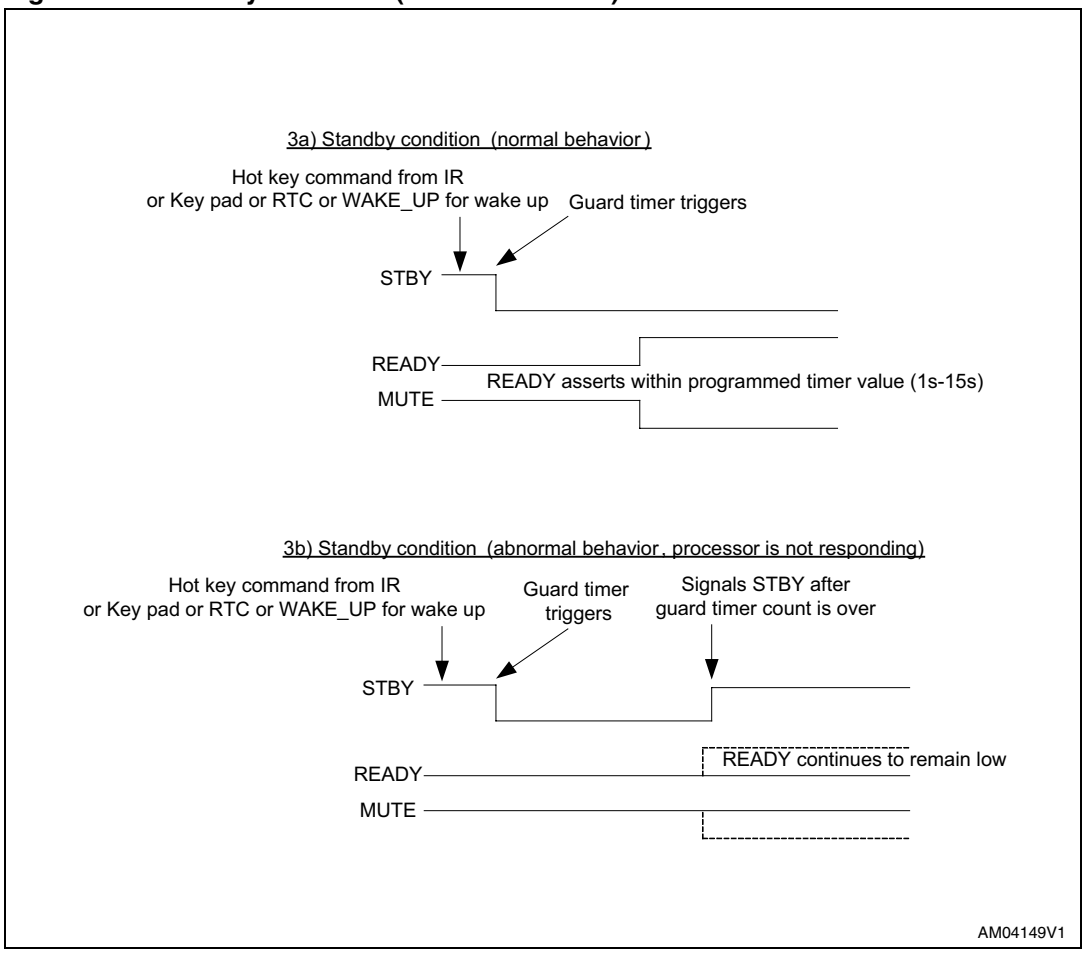
- Guard timer can be kept on during normal condition when READY is high (depending on the user).
- In this condition, the guard timer can be disabled or enabled. If the guard timer is enabled, the timer needs to be cleared before the programmed count of the timer is reached. If the programmed count is reached, the STBY will be asserted.
- It is advisable not to enable the guard timer during normal operation.

3.10.3 Wake-up

The STLED325 can wake-up from any one of the following sources:

- Front-panel keys
- Remote-control keys
- Real time clock (RTC) in 3 conditions (alarm, watchdog timer, oscillator fail)
- External wake-up pin (by a low to high transition on this pin)
- GPIO status changes
- READY pin goes from low to high

Figure 7. Standby condition (normal behavior)



- When the hot-key is detected either from front-panel or remote control or RTC or from a transition (low to high transition) on WAKE_UP pin during stand-by, the STBY pin de-asserts.
- The de-assertion of the STBY triggers the guard timer.
- The timer value is the programmed value by the user (1-15s). If the user did not change the value before entering standby, then it remains 10s.
- Also note that the guard timer is off when the STLED325 is in the standby mode.

The guard timer is thus triggered by a de-assertion of the STBY signal or by internal power on reset signal.

3.11 Real time clock (RTC)

The STLED325 integrates a low power Serial RTC with a built-in 32.768 kHz oscillator (external crystal controlled). Eight bytes of the SRAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 12 bytes of SRAM provide status/ control of alarm and watchdog functions. Addresses and data are transferred serially via a two line, bi-directional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. Note that all 4 digits must be enabled before using the RTC display.

Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts and watchdog timer. The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

The RTC operates as a slave device through the slave address of the STLED325 on the serial bus. Access is obtained by implementing a start condition followed by the correct device slave address. The 16 bytes contained in the device can then be accessed sequentially in the following order:

- 1. Reserved
- 2. Seconds register
- 3. Minutes register
- 4. Hours register
- 5. Day register
- 6. Date register
- 7. Century/month register
- 8. Year register
- 9. Calibration register
- 10. Watchdog register
- 11 - 16. Alarm registers

The RTC keeps track of the date and time. Once the date and time are set, the clock works when the STLED325 is in normal operation and standby operation. Wake-up alarm feature is also included in the RTC module. The accuracy of the RTC is approximately 20 ppm (±50secs/month). How-ever this much depends on the accuracy of the external crystal used.

The wake-up alarm is programmed to wake up once the date and time set are met. This feature is present in normal and standby mode of operation. Only one date and time is available for setting.

The real time clock (RTC) uses an external 32.768 kHz quartz crystal to maintain an accurate internal representation of the second, minute, hour, day, date, month, and year. The RTC has leap-year correction. The clock also corrects for months having fewer than 31 days.

3.11.1 Reading the real time clock

The RTC is read by initiating a Read command and specifying the address corresponding to the register of the real time clock. The RTC registers can then be read in a sequential read mode. Alarms occurring during a read are unaffected by the read operation.

3.11.2 Writing to the real time clock

The time and date may be set by writing to the RTC registers. The new RTC time can be updated by writing to the RTC registers. The new time only takes affect after a complete write cycle. If the write cycle is incomplete, the new time value is discarded. A single byte may be written to the RTC without affecting the other bytes.

3.11.3 Register table for RTC

Table 2. Register table for RTC

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Functional/range BCD format	
00h	Reserved				Reserved					
01h	OSC_ST	10 seconds			Seconds				Seconds	00-59
02h	Rsvd	10 minutes			Minutes				Minutes	00-59
03h	MD_HM_MS		10 hours		Hours (24 hours format)				Hours	00-23
04h	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Day of week			Day	01-7
05h	Rsvd	Rsvd	10 date		Day of month				Date	01-31
06h	CB1	CB0	Rsvd	10M	Month				Century/month	0-3/01-12
07h	10 years				Year				Year	00-99
08h	12/24	Rsvd	Cal_sign	Calibration					Calibration	
09h	RB2	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	Rsvd	ABE	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	RPT6	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDFEn	Alarm: day of week			Rsvd (bypass mode)				Flags	

Legend:

Cal_Sign = Sign bit

OSC_ST = Oscillator Stop bit

BMB0 – BMB4 = watchdog multiplier bits

CB = Century bits

ABE = Alarm in battery back up mode enable bit

AFE = Alarm flag enable

RB0 – RB2 = watchdog resolution bits

RPT1 – RPT6 = alarm repeat mode bits

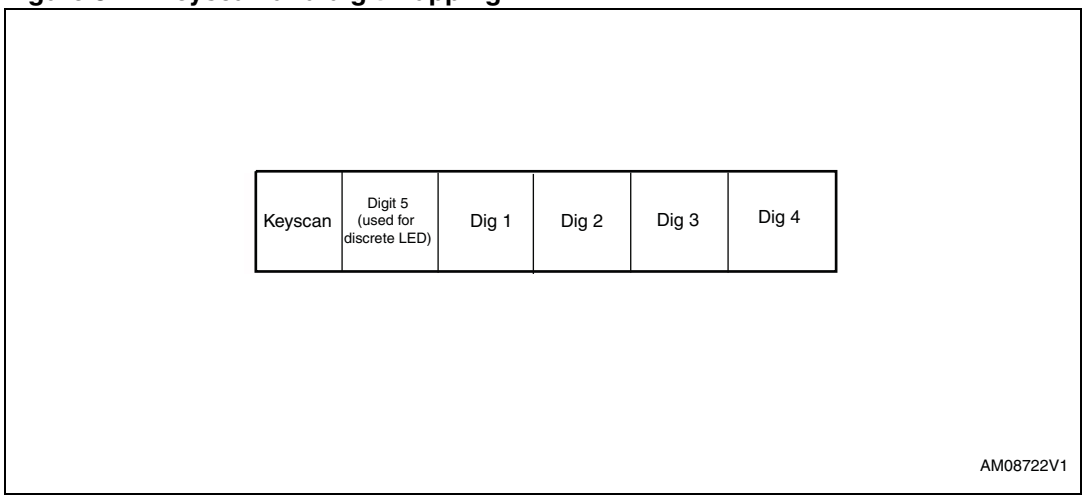
WDFEn = watchdog flag enable

12/24 = 12 hour or 24 hour format (‘0’ for 24-hour format and ‘1’ for 12-hour format). For 12 hour PM display, the 8th segment of last digit (digit 4) is driven to indicate PM mode through a dot on the last digit.

It is recommended to fill the unused bits in the register map to 0 upon a cold boot up. The timekeepers and alarm store data in BCD format, while the calibration, watchdog bits are in binary format.

The structure of the frame is shown below. For RTC, all the Dig1 to Dig4 must be configured to show the proper time.

Figure 8. Keyscan and digit mapping



If the date programmed in the RTC exceeds a valid date value, then the RTC does not function as desired. So the invalid dates should never be programmed into the RTC.

3.11.4 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the STLED325 is in the standby mode to serve as a system wake-up call.

Bits RPT6-RPT1 put the alarm in the repeat mode of operation. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

Note that by default, the alarm repeat mode is enabled and by default the repeat frequency is set to “once per year”.

Address locations 0Ah to 0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time. The default repeat alarm mode is once per year. Programming the RPT[6:1] bits changes the repeat alarm mode.

Table 3. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	RPT6	Repeat alarm mode
1	1	1	1	1	1	Once per week
1	1	1	1	1	0	Once per second
1	1	1	1	0	0	Once per minute
1	1	1	0	0	0	Once per hour
1	1	0	0	0	0	Once per day
1	0	0	0	0	0	Once per month
0	0	0	0	0	0	Once per year

If the RPT value is other than the valid ones listed in the table, the default repeat alarm mode is once per second so as to quickly alert the user of an incorrect alarm setting. When the clock information matches the alarm clock settings based on the match criteria defined by RPT[6:1], then the alarm flag is set. Then if the alarm flag enable bit, is also set, this will activate the alarm interrupt. Interrupt is cleared by reading the Interrupt registers.

3.11.5 Century bits

The clock shall include correction for leap years. The clock shall also correct for months fewer than 31 days. Corrections for 28, 29 (leap year –valid until year 2100), 30, 31 day months must be made automatically.

The two Century bits increment in a binary fashion at the turn of the century, and handles all leap years correctly. See table for additional explanation.

Table 4. Century bits examples

CB[0]	CB[1]	Leap year?	Example (1)
0	0	Yes	2000
0	1	No	2100
1	0	No	2200
1	1	No	2300

1. Leap year occurs every 4 years (for years evenly divisible by 4), except for years evenly divisible by 100. The only exceptions are those years evenly divisible by 400. (The year 2000 was a leap year, year 2100 is not.)

3.11.6 Initial power-on defaults

Upon application of power to the device, the register bits in the RTC initially power-on in the state indicated in table below.

Table 5. Initial power-on defaults

OSC_ST	AFE	WDFEn
0	0	0

Initial power-on defaults value of the RTC registers.

Note: All other control bits power-up in a default state of 0 unless otherwise specified.

3.11.7 Programmable display

The default display of the RTC time is the 2 MSB digit for hour and the 2 LSB digit for minutes. However, if the MD_HM_MS bit is set, then the RTC display for the digits can be changed according to *Table 6*.

Table 6. RTC display

MD_HM_MS	RTC display
10	Date-month
00	Hour-minute (default and recommended)
01	Minute-second
11	Month-date

3.11.8 Lookup table with ppm against the calibration register values

The lookup table of the calibration register values for the equivalent ppm is shown in *Table 7* below:

Table 7. LUT with ppm against the calibration register values

Sign bit	Counts/bit					PPM
0	0	0	0	0	0	0
0	0	0	0	0	1	2
0	0	0	0	1	0	4
0	0	0	0	1	1	6
0	0	0	1	0	0	8
0	0	0	1	0	1	10
0	0	0	1	1	0	12
0	0	0	1	1	1	14
0	0	1	0	0	0	16
0	0	1	0	0	1	18
0	0	1	0	1	0	20
0	0	1	0	1	1	22
0	0	1	1	0	0	24
0	0	1	1	0	1	26
0	0	1	1	1	0	28
0	0	1	1	1	1	31
0	1	0	0	0	0	33
0	1	0	0	0	1	35
0	1	0	0	1	0	37
0	1	0	0	1	1	39
0	1	0	0	0	0	41
0	1	0	0	0	1	43
0	1	0	0	1	0	45
0	1	0	0	1	1	47

Table 7. LUT with ppm against the calibration register values (continued)

Sign bit	Counts/bit					PPM
0	1	1	1	0	0	49
0	1	1	1	0	1	51
0	1	1	1	1	0	53
0	1	1	1	1	1	55
0	1	1	1	0	0	57
0	1	1	1	0	1	59
0	1	1	1	1	0	61
0	1	1	1	1	1	63
1	0	0	0	0	0	0
1	0	0	0	0	1	-4
1	0	0	0	1	0	-8
1	0	0	0	1	1	-12
1	0	0	1	0	0	-16
1	0	0	1	0	1	-20
1	0	0	1	1	0	-24
1	0	0	1	1	1	-28
1	0	1	0	0	0	-33
1	0	1	0	0	1	-37
1	0	1	0	1	0	-41
1	0	1	0	1	1	-45
1	0	1	1	0	0	-49
1	0	1	1	0	1	-53
1	0	1	1	1	0	-57
1	0	1	1	1	1	-61
1	1	0	0	0	0	-65
1	1	0	0	0	1	-69
1	1	0	0	1	0	-73
1	1	0	0	1	1	-77
1	1	0	0	0	0	-81
1	1	0	0	0	1	-85
1	1	0	0	1	0	-90
1	1	0	0	1	1	-94
1	1	1	1	0	0	-98
1	1	1	1	0	1	-102
1	1	1	1	1	0	-106
1	1	1	1	1	1	-110
1	1	1	1	0	0	-114
1	1	1	1	0	1	-118
1	1	1	1	1	0	-122
1	1	1	1	1	1	-126

3.12 Remote control decoder

The remote control (RC) decoder module decodes the signal coming from IR_IN pin. The IR remote control protocols recognized by STLED325 are Philips-RC-5, RCMM, Thomson RCA, R2000, NEC and R-STEP protocols. The selection of remote control protocol to use is done by setting the RC protocols register. The command from the remote control is used to wake-up from standby and resume normal operation. All RC keys can be programmed to act like RC hotkeys. Upon receiving any one of the designated hotkeys, wake-up operation begins.

The address of the appliance (8-bit) is stored first into the internal RAM. Then, the command for the hotkeys is programmed into the internal RAM. Each hotkey memory address could accommodate one byte (8-bit). Usually one byte is reserved for one command. The hot-keys can be configured to wake-up the system by more than one RC device address (up to a maximum of 8 device addresses).

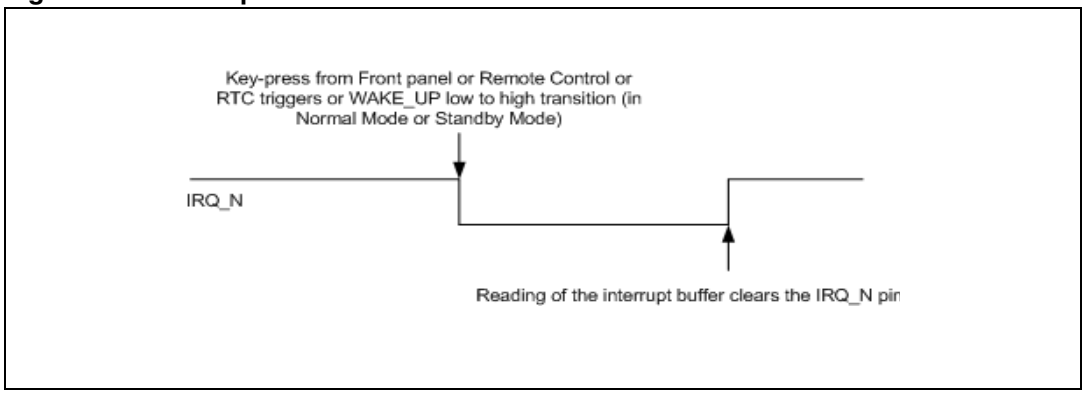
3.13 Interrupt

The STLED325 interrupts the Host by pulling the IRQ_N pin to a low-level both in normal mode of operation and during wake-up. The interrupt is enabled by STLED325 when any of the conditions occur:

- Front panel key press in normal operation or during system standby state
- Remote control key press in normal operation or during system standby state (including the toggle bit changes for all RC protocols)
- A low-to-high on the external pin, WAKE_UP
- Real time clock triggers (alarm, watchdog timer, 32 kHz oscillator fails)
- GPIO input changes
- Low battery indication
- Thermal shutdown

The IRQ_N is an active low level signal and is cleared only after the Interrupt buffer is read. After reading the interrupt buffer, the Host will know the actual source of the interrupt. This allows the Host to exactly know the event which caused the interrupt (e.g STBY key on the Front Panel). The interrupt signal is used to inform the Host of any events detected by the STLED325. Note that the IRQ_N pin is an open-drain pin which requires an external pull-up resistor.

Figure 9. Interrupt



The interrupt output is of active low level type.

While the interrupt is being read by the MCU and a new GPIO or key data comes in, no new interrupt is generated but the register for GPIO and KEY data is updated so that the MCU does not miss the new KEY and GPIO data.

3.14 Ready

The STLED325 supports cutting-off power to the main board for standby operation for good power management. STBY will be set to high when the READY transitions from high to low. During a cold boot up or wake up from standby, if the READY pin stays low, the STLED325 will assert the STBY when the guard timer has finished counting down to 0.

When the READY drops to a low, MUTE goes high immediately and soon after (2µs minimum) the STBY is asserted.

In the normal mode of operation, when READY is a high, the STBY is asserted only when the guard timer is enabled and has finished counting down to 0. This is meant to put the system into stand-by as the READY pin was stuck at high and the guard timer register was not cleared before it finished counting down to 0. It is advised to disable the guard timer during normal operation.

3.15 Mute

The MUTE pin will be set to logic high to mute the audio output before power is cut to the host processor. In wake up mode, the MUTE pin will be set to logic low to enable the audio output immediately after the high assertion of the READY pin. In general, MUTE follows READY pin with an inverted polarity. This pin is used to prevent pop-up sound during power-up and power-down states.

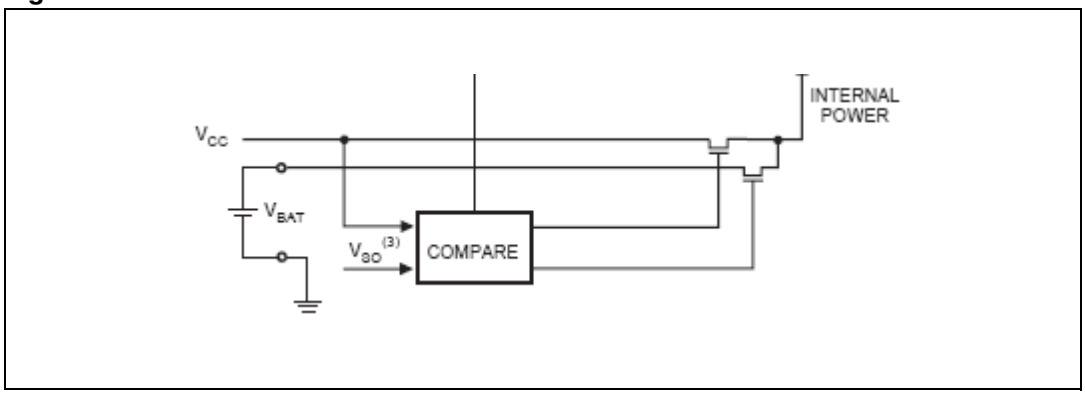
3.16 GPIO

The STLED325 supports 2 additional GPIOs that can be configured as inputs or outputs. As an input, the GPIO can be used to interface to a sensor or a switch or key and as an output, the GPIO can be used to drive individual indicator LEDs.

3.17 Power sense circuits

The STLED325 has a built-in power sense circuit which detects power failures and automatically switches to the battery or super-cap supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by small lithium button supply or a super-cap when a power failure occurs. When operating from the battery or super-cap, all the inputs and outputs are driven to a known state (generally L).

Figure 10. Power sense circuit



For the STLED325 itself, there is the normal operational mode where the supply is from the 5 V V_{CC}. When the V_{CC} drops below a pre-defined low level, the supply source is switched from the V_{CC} to the battery or super-cap supply.

To conserve power and maintain long battery life in this battery supply mode, only the RTC and the clock to the RTC remain operational.

1. The system will only go into battery mode while:

   Vcc < 3.5 V and Vcc < Vbat.

So, it means that the system will only switch to battery mode when Vcc drop below 3.5V and Battery voltage is higher V_{CC} voltage.

2. The system will enter back into Vcc mode from battery mode while:

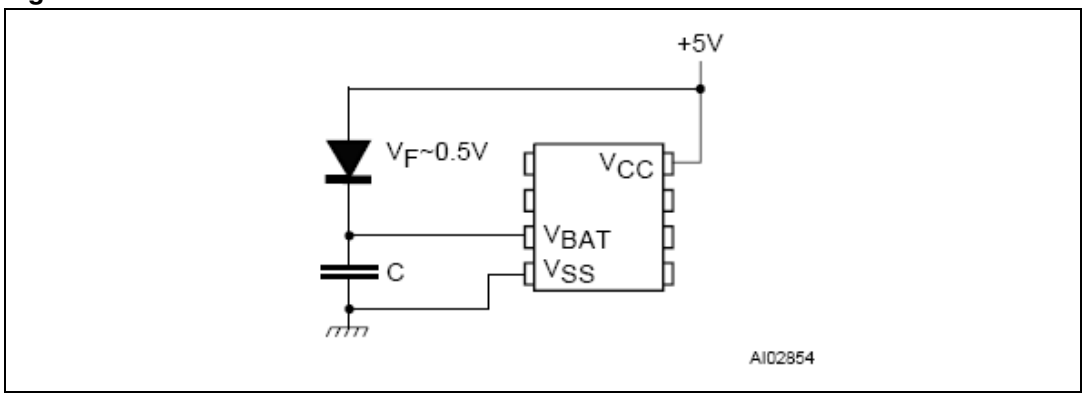
   $V_{CC} > V_{bat}$

It means that the system will switch back to Vcc mode as soon as the V_{CC} is higher than Vbat.

The STLED325 continually monitors Vcc for an out-of-tolerance condition. Should V_{CC} fall below the Switchover voltage (V_{SO} = 3.5 V), the device goes into a low-power mode. Inputs to the device will not be recognized at this time to prevent any erroneous data or outcome from device. The device also automatically switches over to the battery and powers down into an ultra low current mode of operation to maximize the super-cap or battery duration. As system power returns and V_{CC} rises above Vbat, the battery or super-cap is disconnected and the power supply is switched to the external V_{CC}. During the battery or super-cap back-up mode, the clock registers of RTC are maintained by the attached battery or super-cap. On power-up, when V_{CC} returns to a nominal value, write protection continues for t_{REC} (refer to timing diagram in later part of spec).

Upon power-up, the device switches from battery to V_{CC} when V_{CC} > Vbat. When V_{CC} rises above Vbat, it will recognize the inputs.

Figure 11. Circuit



The minimum operating voltage of STLED325 is 2.5 V with a typical VBAT voltage of VCC-VF (diode). Therefore, the typical delta voltage swing across the capacitor is

$\Delta V = V_{CC} - V_F - V_{CCmin}$

where V_F is approximately 0.5 V. Therefore,

$\Delta V = 5 - 0.5 - 2.5 = 2$ V

Since the typical battery current (IBAT) is limited to 7 µA, the capacitance and duration of power-out time can be calculated using the formula:

$I = C\Delta V/\Delta t$

Where I = 7µA, ΔV=2V, C= capacitance in Farads and Δt is power-out time in seconds. Using a 0.1F super-cap, for example, the equation would be:

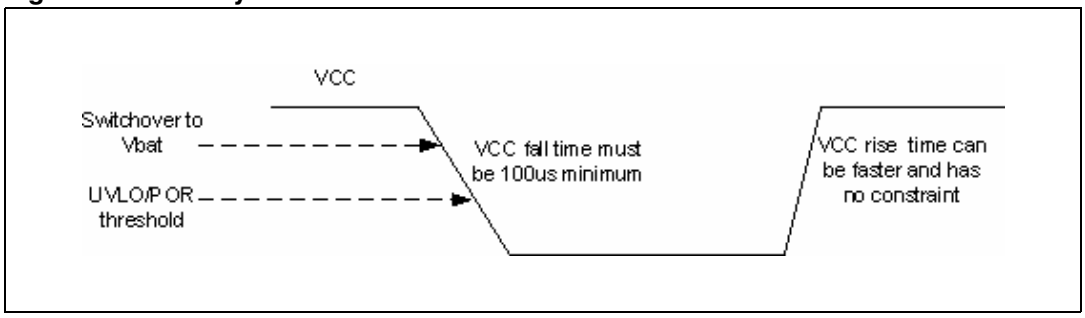
$7\mu A = 0.1F \times 2V/\Delta t$

Solving for Δt, the typical power-down time is about 28,571 seconds = 8 hours.

3.17.1 Switchover

During the period the V_{CC} falls, in order for the battery switchover circuit to work reliably, the fall time of V_{CC} from 5V to 0V should be at least 100µs. This is to allow the comparator to trigger and switch from V_{CC} to V_{BAT} mode should there be a need. During the V_{CC} rise period from 0V to 5V, the rise time of V_{CC} is not critical. This is indicated by the *Figure 12.*

Figure 12. Battery switchover waveform



Also note that for battery operation, there will be a current spike of 5mA in 10us into the battery when V_{CC} to V_{BAT} switchover happens. From V_{BAT} to V_{CC} switching, the current

spike is very low into the battery. The battery must be protected against such spikes. This is not relevant for super-cap.

During the switching from V_{BAT} to V_{CC}, the I2C is active after a minimum of 5ms.

3.17.2 Battery low warning

The STLED325 automatically performs battery voltage monitoring upon power-up. If the interrupt for this condition (ABE) is enabled, the RTC will generate an interrupt pulse if the battery voltage is found to be less than a minimum of 2.5V. However, this condition is unlikely to go away very quickly as time is needed for the battery to be replaced, and it is not desirable to keep issuing an interrupt.

Therefore when this bit is set, this condition is checked once every week. If the condition is still true, then interrupt is sent again.

The ABE bit is an enable bit for battery status check. If the ABE bit was set and the battery low is generated during a power up sequence, this indicates that the battery is below approximately 2.5 V and may not be able to maintain data integrity. At this point, a fresh battery needs to be installed or the super-cap recharged.

This situation only occurs when a battery is used but not with a super-cap as the super-cap re-charges when the supply is present.

3.17.3 Different power operation modes

The device is capable to support the different power modes as shown in the *Table 8.*

Table 8. Different power operation modes

V_{CC}	V_{BAT}	Condition	Operation
Present	Present	$V_{CC} > V_{BAT}$	Normal operation of chip from V_{CC}
Present	Absent (Float or 0V)	$V_{CC} > V_{BAT}$ and $V_{CC} > 3.5V$	Normal operation of chip from V_{CC} until V_{CC} is 3.5V
Absent (Float or 0V)	Present	$V_{BAT} > 2.5V$	Chip operations from V_{BAT} in a low power mode of operation
$V_{CC} < 3.5V$	$V_{BAT} > V_{CC}$		Chip operations from V_{BAT} in a low power mode of operation
Absent (Float or 0V)	Absent (Float or 0V)	$V_{CC} < 3.5V$ and $V_{BAT} < 2.5V$	Chip does not function. Completely shutdown.

3.18 Bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage (typical voltage is 3.3 V) via a pull-up resistor (typical value is 10 K). The following protocol has been defined.

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High.
- Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain High.

Start data transfer: A change in the state of the data line, from high to Low, while the clock is High, defines the START condition.

Stop data transfer: A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.
Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit. By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

Acknowledge: Each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the master transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Note: Refer to Philips I^2C specification or contact STMicroelectronics for more information on I^2C.

Table 9. Pin description

Pin number	Symbol	Type	Name and function
1	MUTE	OUT	Output from the STLED325 to gracefully mute the audio before entering standby mode
2	IRQ_N	OUT	Interrupt output (active low level type) to interrupt the MCU under various conditions
3	GPIO0	IN/OUT	GPIO0 that can be configured as an input or output
4	GPIO1	IN/OUT	GPIO1 that can be configured as an input or output
5	IR_IN	IN	Remote control data input
6	SDA	IN/OUT	I^2C compatible serial data I/O
7	SCL	IN	I^2C compatible serial clock input
8	WAKE_UP	Input	Wake-up pin (can be used for wake-up on detecting a low to high transition). AV wake-up or CEC wake-up.
9	DIG5	OUT	Digit output pin. Can be used in conjunction with 8 segment outputs to control 8 discrete LEDs on the front panel.
10 - 13	DIG4 –DIG1	OUT	Digit output pins
14	VCC	PWR	5.0 V ± 10% main supply voltage. Bypass to GND through a 0.1 µF capacitor as close to the pin as possible.
15, 16	KEY2-KEY1	IN	Input data to these pins from external keyboard are latched at end of the display cycle (maximum keyboard size is 8 x 2). 5V digital input.
17 - 24	SEG8/KS8 to SEG1/KS1	OUT	Segment output pins (dual function as key source)
25	ISET	IN	Current sense input. Connect resistor to ground to set constant current through LEDs. Connect to GND through a resistor to set the peak segment current.
26	VBAT	Input	Battery power supply for the RTC when there is no supply to the chip
27	VREG	Output	1.8V regulator output. Connect to an external capacitor.
28	GND	PWR	Connect this pin to system GND
29	XIN	IN	Connect to an external crystal or apply external clock
30	XOUT	OUT	Output of the external crystal. Open when external clock
31	STBY	OUT	Hardware pin to control the power to the Host
32	READY	IN	Input to the device from the Host to indicate that Host is ready
EPAD			Exposed pad. Connect to PCB GND.

4 Electrical ratings

4.1 Absolute maximum ratings (T_A = 25 °C, GND = 0 V)

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages are referenced to GND.

Table 10. Absolute maximum ratings (T_A = 25 °C, GND = 0 V)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage to ground		-0.5 to +7.0	V
V_I	Logic input voltage (KEY1, KEY2 inputs)		-0.5 to +7.0	V
V_I	Logic input voltage (all input pins except KEY1, KEY2)		-0.5 to +3.6	V
P_D	Power dissipation[1]		1200	mW
T_A	Operating ambient temperature		-40 to 85	°C
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature		-65 to +150	°C
T_L	Lead temperature (10 sec)		300	°C
V_{ESD}	Electrostatic discharge voltage on all pins[2]	Human body model	-2 to +2	kV

Table 11. Thermal data

Symbol	Parameter	QFN 32	Unit
$R_{Tj\text{-}c}$	Thermal resistance junction-case	TBD	°C/W

4.2 Recommended operating conditions

4.2.1 DC electrical characteristics

(T_A = -40 to +85 °C, V_{CC} = 5.0 V ± 10%, GND = 0 V)

Table 12. DC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	External supply voltage		4.5	5.0	5.5	V
V_{REG}	Internal logic supply voltage and regulator output		1.62	1.8	1.98	V
V_{IH}	HIGH level input voltage (all digital pins except KEY1 and KEY2)	High level guaranteed	1.35		1.98	V
V_{IL}	LOW level input voltage (all digital pins except KEY1 and KEY2)	Low level guaranteed	0		0.45	V
V_{IH}	HIGH level input voltage (KEY1 and KEY2 pins)	High level guaranteed	3		5.5	V
V_{IL}	LOW level input voltage (KEY1 and KEY2 pins)	Low level guaranteed	0		2	V
I_{IH}, I_{IL}	Input current (all pins)	$V_{IN} = V_{IH}$ or V_{IL}	-2		2	µA
V_{HYS}	Hysteresis voltage (digital pins)			0.2		V
V_{OL}	Low level output voltage (Digital output pins)	I_{OL2} = 4 mA			0.4	V
I_{OLEAK}	Driver leakage current	Drivers off			-150	µA
I_{SEG}	Segment drive LED sink current	$V_{LED} = V_F$ = 2.5 V $V_{DIGIT} = V_{CC} - 1.0$	-30	-40	-50	mA
I_{DIG}	Digit drive LED source current	$V_{DIGIT} = V_{CC} - 1.0$	240	320	400	mA
I_{TOLSEG}	Segment drive current matching	V_{CC}=5.0 V, T_A=25°C V_{LED}=2.5V; LED current = 40 mA			±4.0	%
R_{SET}	External current setting reference resistor (precision = ±1% tolerance)	I_{SEG} = 40 mA		360		Ω

4.3 Power consumption estimation

Each port of the STLED325 can sink a maximum current of 40 mA into an LED with a 3.4 V forward voltage drop when operated from a supply voltage of 5.0 V. The minimum voltage drop across the internal LED drivers is thus 5.0 - 3.4 = 1.6 V. The STLED325 can sink 8 x 40 = 320 mA when all outputs are operating as LED segment drivers at full current. On a 5.0 V supply, a STLED325 dissipates (5.0 V-3.4 V) x 320 mA = 512 mW when driving 8 of these 3.4 V forward voltage drop LEDs at full current. If the application requires high drive current, consider adding a series resistor to each LED to drop excessive drive voltage off-chip.

If the forward voltage of the LED is lesser than 4.4 V (say 2.4 V), then the maximum power dissipation of STLED325 when all segments are turned on will be (5 - 2.4) V x 320 mA = 832 mW. To lower the power dissipation, consider adding a small series resistor in the supply. Another alternative is to in-crease the value of the RSET to lower the current of the LEDs from 40 mA to say 30 or 20 mA.

The efficiency will be the power consumption in the LEDs divided by the input power consumed.

Equation 1 Efficiency = Vdiode x Idiode / V_{CC} x I_{CC}

As an example, consider LED with forward voltage of VF = 2.4 V, Ipeak = 40 mA, VCC (max) = 5.5 V, N=number of segments=8(max), D=duty cycle=15/16,

Power dissipation, PD (max) = 5 mA x 5.5 V + (5.5-2.4) V x (15/16) x 40 mA x 8 = 27.5 + 780 = 807.5 mW. To lower this value, add a series resistor with the supply.

Table 13. Voltage drop estimation with RGB LED

LED	Typical forward voltage VF	Typical current	Typical supply voltage	Digit driver drop	External VF	Segment driver drop
Red	2.2 V	40 mA	5 V	1 V	2.2 V	1.8
Green	2.5 V	40 mA	5 V	1 V	2.5 V	1.5
Blue	3 V	40 mA	5 V	1 V	3 V	1 V

Note that the above analysis is for a typical condition. If the VF is higher and the supply voltage is lower than 5V, then it is recommended to operate the LED at a lower current than 40mA in order to have enough headroom for the digit and segment drivers so as not to affect the brightness and matching.

Table 14. Capacitance (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance (all digital pins)				15	pF

Table 15. Power supply characteristics (T_A = -40 to 85°C)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{CC}	Operating power supply current	All blocks of chip ON except that no display load V_{CC} = 5.5V			TBD	mA
$I_{CC(Q)}$	Quiescent supply current	Display OFF V_{CC} = 5.5V			2	mA

)

Table 16. Dynamic switching characteristics (T_A = -40 to +85 °C, V_{CC} = 5.0V ± 10%, GND=0.0V, Typical values are at 25°C)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
tHD:STA	START condition hold time (after this period the first clock pulse is generated)	600			ns
tSU:STA	START condition setup time (only relevant for a repeated start condition)	600			ns
tSU:DAT	Data setup time*	100			ns
tHD:DAT	Data hold time	0			µs
tSU:STO	STOP condition setup time	600			ns
tBUF	Time the bus must be free before a new transmission can start	1.3			µs
trec	Watchdog output pulse width	96		98	ms

Note: The transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of the SCL.

Table 17. Timing characteristics (T_A = -40 to +85 °C, V_{CC} = 5.0 V ± 10%, GND=0.0 V, typical values are at 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Propagation delay time	t_{PLZ}			300	ns	CLK -> SDA C_L = 15 pF, R_L = 10 kΩ	
	t_{PZL}			100	ns		
Rise time	t_{TZH1}			2	µs	C_L = 300 pF	Seg1 to Seg12
							Grid1 to Grid8, Seg13/Grid16 to Seg20/Grid9
	t_{TZH2}			0.5	µs		
Fall time	t_{THZ}			120	µs	C_L = 300 pF, Segn, Dign	
Input capacitance	C_I			15	pF		
Mute active to standby active	T_{M-S}	2			µs		
GPIO edge to interrupt trigger	T_{irq}		8		µs		

4.4 Oscillator and crystal characteristics

Table 18. Oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{STA}	Oscillator start voltage	≤10 seconds	1.5			V
tSTA	Oscillator start time	V_{CC} = 3.0 V			1	s
CL1	X_{IN}				25	pF
CL2	X_{OUT}				25	pF
	IC-to-IC frequency variation(1)		-20		+20	Ppm

1. Reference value. T_A = 25 deg C, V_{CC} = 3.0 V, CFM-145 (C_L = 6 pF, 32.768 KHz) manufactured by Citizen.

Table 19. Crystal electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fo	Resonant frequency(1)			32.768		KHz
Rs	Series resistance(2)			35	40(3)	kΩ
CL	Load capacitance			12.5		pF

1. Externally supplied. ST recommends the Citizen CFS-145 (1.5 x 5 mm) and the KDS DT-38 (3 x 8 mm) for thru-hole, or the KDS DMX-26S(3.2x8mm) for surface-mount, tuning fork-type quartz crystals. KDS can be contacted at kouhou@kdsj.co.jp or http://www.kdsj.co.jp. Citizen can be contacted at csd@citizen-americal.com or http://www.citizencrystal.com
2. Circuit board layout considerations for the 32.768KHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

Note: 1 Oscillator is not production tested.

2 Externally supplied. ST recommends the Citizen CFS-145 (1.5 x 5 mm) and the KDS DT-38 (3 x 8 mm) for thru-hole, or the KDS DMX-26S(3.2x8mm) for surface-mount, tuning fork-type quartz crystals. KDS can be contacted at kouhou@kdsj.co.jp or http://www.kdsj.co.jp Citizen can be contacted at csd@citizen-americal.com or http://www.citizencrystal.com

3 Circuit board layout considerations for the 32.768KHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

4 Guaranteed by design.

4.5 ESD performance

Table 20. ESD performance

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ESD	MIL STD 883 method 3015 (all pins)	HBM		±2		kV

Table 21. Battery range and battery detect

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT(1)	Battery supply voltage		2.5	3	3.5(2)	V
I_{BAT}	Battery supply current	T_A= 25 C, V_{CC}= 0 V, Oscillator ON, V_{BAT}=3 V		7	10	uA

1. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.
2. For rechargeable back-up, V_{BAT}(max) may be considered V_{CC}.

Figure 13. Power down/up mode ac waveforms

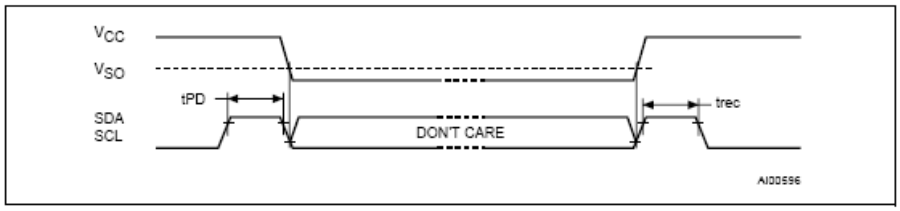


Table 22. Power down/up AC characteristics

Symbol	Parameter (1)(2)	Min	Typ	Max	Unit
tpD	SCL and SDA at V_{IH} before power down	0			ns
trec	SCL and SDA at V_{IH} after power-up	10			µs

1. V_{CC} fall time should not exceed 5mV/µs.
2. Valid for ambient operating temperature: T_A=-40 to 85, V_{CC} = 2.5V to 5.5V (except where noted)

Table 23. Power down/up trip points DC characteristics

Symbol	Parameter(1)(2)	Min	Typ	Max	Unit
V_{SO}	Battery back-up switchover voltage (from V_{CC} to V_{BAT})		V_{CC} < 3.5V and V_{CC} < V_{BAT}		V
V_{SO}	Battery back-up switchover voltage (from V_{BAT} to V_{CC})		V_{CC} > V_{BAT}		V

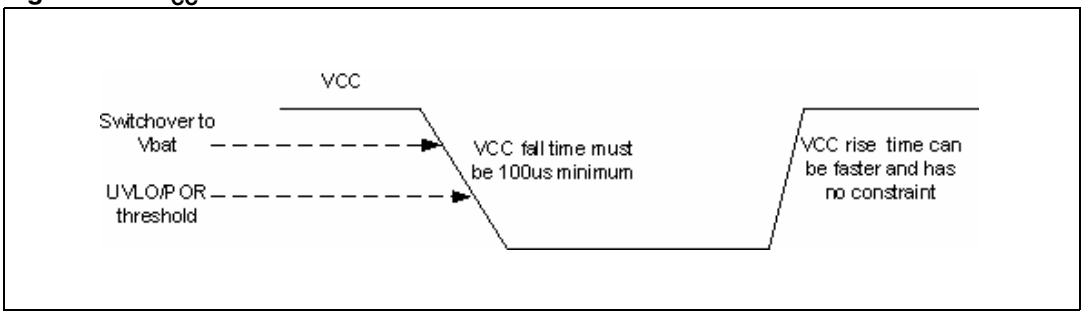
1. All voltages are referenced to GND.
2. Valid for ambient operating temperature: T_A=-40 to 85, V_{CC} = 2.5V to 5.5V (except where noted)

Table 24. Thermal shutdown characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TSD	Thermal shutdown threshold	VCC=5V		140		Deg C
THYS	Hysteresis	VCC=5V		15		Deg C

1. Thermal shutdown is not production tested.

Figure 14. V_{CC} characteristics



5 Display RAM address and display mode

The display RAM stores the data transmitted from an external device to the STLED325 through the serial interface. The addresses are as follows, in 8-bits unit:

Table 25. Bit map for segment 1 to segment 8

Seg1	Seg4	Seg8
10 H_L	10 H_U	Dig1
11 H_L	11 H_U	Dig2
12 H_L	12 H_U	Dig3
13 H_L	13 H_U	Dig4
14 H_L	14 H_U	Dig5

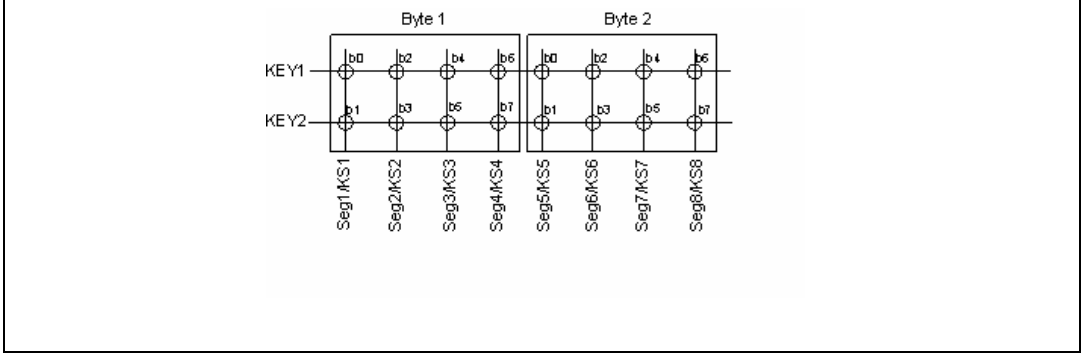
b0	b3	b4	b7
XX H_L		XX H_U	

“0” in memory means GND on outpu; ‘1” in memory means V_{CC} on output.

6 KEY matrix and key-input data storage RAM

The key matrix is of 8x2 configuration, as shown below:

Figure 15. KEY matrix and key-input data storage RAM



The data of each key are stored as illustrated below, and are read by the appropriate read command, starting from the least significant bit.

Key 1	Key 2	Key 1	Key 2	Key 1	Key 2	Key 1	Key 2
Seg1	KS1	Seg2	KS2	Seg3	KS3	Seg4	KS4
Seg5	KS5	Seg6	KS6	Seg7	KS7	Seg8	KS8
b0	**b1**	**b2**	**b3**	**b4**	**b5**	**b6**	**b7**

All the front panel keys can be configured as hot keys using the “configuration mode setting command”. Alternatively, any number of keys out of 16 keys can be programmed for hot key functions by using the hot-key setting command.

It is recommended to read the hot key values immediately upon STBY de-assertion. If they are not read within the guard preset timer value, the hot key data are cleared.

It is recommended to have 10 KΩ pull down resistors on the KEY1 and KEY2 input pins and the output SEG/KS pins can see a maximum load of 300pF. This load condition is important for the key dis-charge cycle time.

7 Commands

A command sets the display mode and status of the LED driver.

The first 1 byte input to the STLED325 through the SDA pin after the slave address is regarded as a command. If slave address is not transmitted before the commands/data are transmitted, the commands/data being transmitted are invalid (however, the commands/data already transmitted remain valid).

7.1 Configuration mode setting command

This command initializes the STLED325 and performs any one of the following functions:

i) Selects the duty factor (1/8 to 1/16 duty factor). When this command is executed, display is turned off. To resume display, the display ON command must be executed. If the same mode is selected, nothing is performed.

ii) Selects the remote control protocol to use.

iii) Sets the guard timer. The guard timer is configurable from 1 to 15s or turned off completely.

iv) Sets the guard timer action to perform when the guard timer counts. Two actions are allowed: no action or set STBY to high level.

MSB							LSB
0	0	b5	b4	b3	b2	b1	b0

Bits b7-b6 = 00 is decoded as a configuration mode setting command. The subsequent bits are de-coded as follows:

b5: enables wake-up from the external WAKE_UP pin

b4: enable for the display configuration setting change (number of digits)

b3: allows display of RTC (during normal or STBY modes)

b2: enables all RC keys as hot-keys

b1: enables all FPK keys as hot-keys

b0: enables the Guard Timer to issue STBY once the timer expires

Note: When displaying the RTC during normal mode, if the µP is writing data to STLED325 using I^2C bus, the RTC display on LED momentarily turns off.

The first byte after the configuration command is in the following format:

MSB							LSB
b7	b6	b5	b4	B3	b2	b1	b0

Remote control protocol setting (bits b6-b4)

000: RC Disabled (default)

001: Philips RC-6 (optional only enabled for Philips)

010: Philips RC-5

011: Philips RCMM

100: NEC

101: R-STEP

110: Thomson R2000

111: Thomson RCA

When b7='0', incoming RC data is output on SDA in decoded format where the Device Address, Start Bit, Toggle Bit and Data Bits are sent. Note that the default location is 0x00 for the first device address. This order of the bits sent is in the same format as the incoming RC data.

When b7='1', incoming raw data (no header information) is output on SDA.

Address decoding is still performed to decode the corresponding RC protocol. The format of the data on SDA corresponds to the format of the respective RC frame.

For details, refer to the RC protocol section of the datasheet.

GUARD TIMER SETTING (bits b3-b0)

0000: Turned off (guard timer disabled)

0001: 1 seconds

0010: 2 seconds

1111: 15 seconds

The second byte after the configuration command is in the following format:

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

7-Segment display mode setting (bits b1-b0)

00: 1 digit, 8 segments (Digit 1 pin output is enabled)

01: 2 digits, 8 segments (Digit 1 and Digit 2 pin outputs are enabled)

10: 3 digits, 8 segments (Digit 1, Digit 2 and Digit 3 outputs are enabled)

11: 4 digits, 8 segments (Digit 1, Digit 2, Digit 3 and Digit 4 outputs are enabled)

b2: configuration for the digital outputs of the chip

b2 = 1 will enable the outputs of the chip to be push pull type to 1.8V

b2 = 0 will enable the outputs of the chip to be open-drain (can be externally pulled up to 3.3V)

b3: configuration for the GPIO0

b3 = 0 enables the GPIO0 as input

b3 = 1 enables the GPIO0 as output

b4: configuration for the GPIO1

b4 = 0 enables the GPIO1 as input

b4 = 1 enables the GPIO1 as output

b5 = interrupt enable register bit for GPIO (applies to both GPIO0 and GPIO1)

b5 = 0 disables the interrupt generation from any of the two GPIOs

b5 = 1 enables the interrupt generation from any of the two GPIOs inputs change

b6 = configuration of the edge trigger for GPIO0 (works only when b5 is enabled)

b6 = 0 sends interrupt when GPIO0 triggers from a high to a low

b6 = 1 sends interrupt when GPIO0 triggers from a low to a high

b7 = configuration of the edge trigger for GPIO1 (works only when b5 is enabled)

b7 = 0 sends interrupt when GPIO1 triggers from a high to a low

b7 = 1 sends interrupt when GPIO1 triggers from a low to a high

The minimum pulse width for a valid GPIO detection must be 8us minimum.

Upon power application, the following modes are selected:

Display mode setting: the 4-digit, 8-segment mode is selected (default: display off and keyscan on).

Remote control protocol setting: RC-5.

Guard timer setting: turned on with 10s. After the first command is processed by STLED325, the guard timer is turned off until it is turned on by the host.

Guard timer action: Issue Standby.

7.2 Data setting command

This command sets the data-write and data-read modes.

MSB							LSB
0	1	b5	b4	b3	b2	b1	b0

Description: Bits b7-b6 = 01 is decoded as a data setting command. The subsequent bits are decoded as follows:

b5 b4 = 00: data write command (see bits b1-b0)
b5 b4 = 01: data write 1 command (see bits b1-b0)
b5 b4 = 10: data read 1 command (see bits b1-b0)
b5 b4 = 11: data read 3 command (see bits b1-b0)

b3: clear the guard timer (no change in guard time)

b2: when set to a 1, the guard timer is forced to enable and starts the count again.

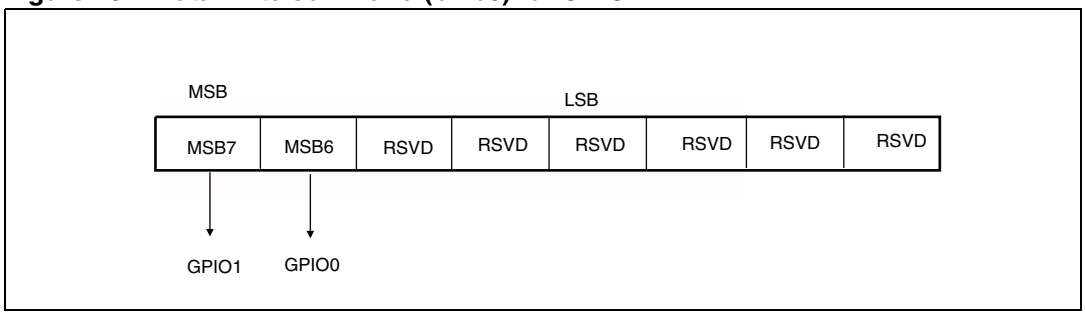
While in normal mode, the count starts

Table 26. Data write command. b5 b4: 00

b1-b0	
00	Write memory (display or RTC) – Address range: 0x00-0x0F. Start address pointer location is 0x00.
01	Write memory (display). Address range: 0x10-0x13. Start ad-dress pointer location is 0x10.
10	Write memory (discrete LED). Address: 0x14.
11	Write data into GPIOs if they are configured as outputs (see note 1)

Note 1: The following byte with MSB7 and MSB6 corresponds to GPIO[1:0] for data to be written into GPIO1 and GPIO0 when they are configured as outputs.

Figure 16. Data write command (b7 b6) for GPIO



When b7 is 1, it drives logic 1 on GPIO1 output and when it is 0, it drives logic 0 on GPIO1 output.

When b6 is 1, it drives logic 1 on GPIO0 output and when it is 0, it drives logic 0 on GPIO0 output.

Table 27. Data Write 2 command. B5 b4: 01

B1-b0	
00	Reserved
01	Reserved (RC6 disable)
10	Reserved (RC6 enable)
11	Enter standby mode

Any subsequent data bytes in this case will be ignored.

Table 28. Data Read 1 command. b5 b4: 10

b1-b0	
00	Read Key (following 2 bytes will contain key data)
01	Read GPIO register (following 1 byte will contain the GPIO data with MSB7: GPIO1 data and MSB6: GPIO0 data). This is the input monitor for GPIO[1:0] for reading purpose. When b7 of subsequent byte is low, it means that GPIO1 input is low and when it is high, it means that GPIO1 input is high. When b6 of subsequent byte is low, it means that GPIO0 input is low and when it is high, it means that GPIO0 input is high.
10	Read RC data (following four bytes are the address + command bytes from RC)
11	Read Interrupt status register (refer to the Interrupt Flag section for detailed description)

Table 29. Data Read 2 command. b5 b4: 11

b1-b0	
00	Reserved
01	Read configuration byte values (see section on configuration bytes)
10	Read LED display memory
11	Read RTC memory. Address command must be issued prior to reading.

On power application, the normal operation mode and address increment mode is set with the default display memory address set to 0x10 (start of display memory address location). Refer to the display memory section.

In the auto increment address mode, the address command is sent once followed by the data bytes.

Alternatively, the data command can be sent followed by the data bytes. In this case, when new display data is to be written, the last value of the address will be used and then incremented. Upon reaching the last display memory address, the address jumps to 0x10, as it represents the first address location of the display memory.

In fixed address mode, the address command has to be sent followed by the display data. When next byte of data is to be written, address command has to be sent again before new display data byte.

When the user wants to read the RTC data from the specified memory location of RTC, the user must first set the address of the RTC location using “Address Setting Command” after which send the “Read RTC Register” command.

If the address pointer was located in the display memory location and user issues a “Read RTC Register” command without sending the “Address Setting Command”, the RTC data is read from the address location of the previous value of the RTC address pointer.

Thus before reading the RTC register data, the user must set the proper address for RTC using “Address Setting Command”.

Prior to writing data to the RTC registers, the address of the RTC must be set using the Address Setting command. Else, if the address pointer happens to be pointing at the LED display memory, then the data will be written to the address location of the previous value in the RTC address pointer. This is vice-versa true for the LED display memory.

7.3 Configuration data

Up to a maximum of 5-bytes are sent from LSB to MSB as configuration data. The 29-bytes represent the following configuration information:

MSB (b7) LSB (b0)

Byte1							
B7	B6	B5	B4	B3	B2	B1	B0
Decoded/Raw RC setting	RC Protocol setting			Guard timer setting			
Byte 2							
B7	B6	B5	B4	B3	B2	B1	B0
Interrupt config for GPIO1	Interrupt config for GPIO0	Interrupt enable config for GPIOs	GPIO1 configuration (input or output)	GPIO0 configuration (input or output)	Digit 5 discrete LED config	7-segment LED display configuration setting	
Byte 3							
B7	B6	B5	B4	B3	B2	B1	B0
Not used			For display enable	For display dimming setting			
Byte 4							
Front Panel Hot Key Bank 1							
Byte 5							
Front Panel Hot Key Bank 2							

On power application, the normal operation mode and address increment mode is set with the default display memory address set to 0x10 (start of display memory address location). Refer to the display memory section.

In the auto increment address mode, the address command is sent once followed by the data bytes.

Alternatively, the data command can be sent followed by the data bytes. In this case, when new display data is to be written, the last value of the address will be used and then

incremented. Upon reaching the last display memory address, the address jumps to 0x10, as it represents the first address location of the display memory.

In fixed address mode, the address command has to be sent followed by the display data. When next byte of data is to be written, address command has to be sent again before new display data byte.

When the user wants to read the RTC data from the specified memory location of RTC, the user must first set the address of the RTC location using “Address Setting Command” after which send the “Read RTC Register” command.

If the address pointer was located in the display memory location and user issues a “Read RTC Register” command without sending the “Address Setting Command”, the RTC data is read from the ad-dress location of the previous value of the RTC address pointer.

Thus before reading the RTC register data, the user must set the proper address for RTC using “Address Setting Command”.

Prior to writing data to the RTC registers, the address of the RTC must be set using the Address Setting command. Else, if the address pointer happens to be pointing at the LED display memory, then the data will be written to the address location of the previous value in the RTC address pointer. This is vice-versa true for the LED display memory.

7.3.1 Interrupt flags

The interrupt is sent on the IRQ_N pin when any one of the event occurs (FP key pressed, RC key pressed or preset value of RTC/guard timer is triggered or activity on WAKE_UP pin or GPIO pins). Simultaneously, the interrupt flags are set. The micro-processor can read the interrupt flags by send-ing the read interrupt flag register command. The following 16-bit data is read by the processor after sending this command. This enables the microprocessor to know what caused the interrupt to occur. If the host sees an interrupt issued from first byte, it is not necessary to read the second byte.

Figure 17. Interrupt bit mapping in Byte 1

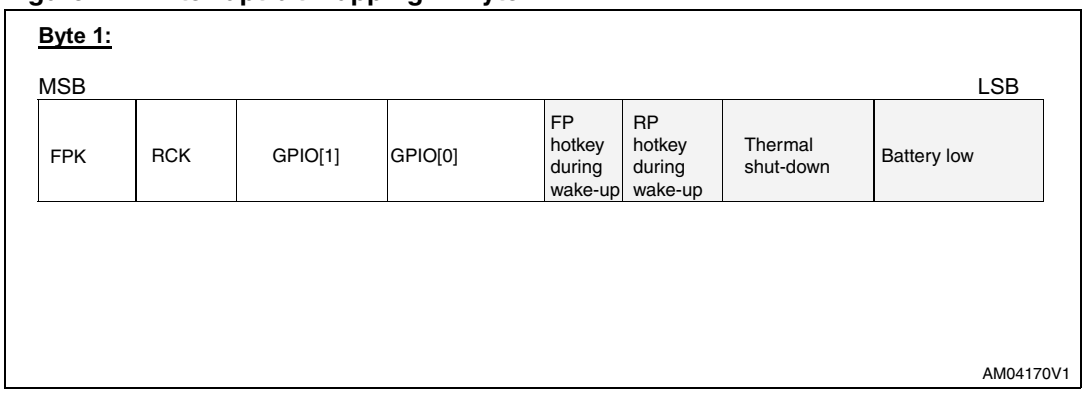
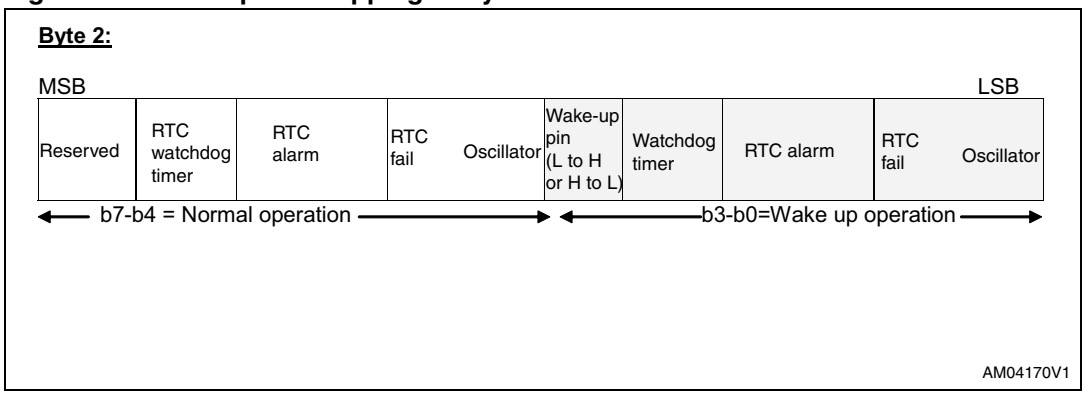


Figure 18. Interrupt bit mapping in Byte 2



In the normal mode of operation, when any FP or RC key is pressed or when alarm/watchdog is triggered, the STLED325 sets the flags in the above interrupt flag register and asserts the IRQ_N pin. The data which caused the interrupt to assert remains in the buffer until it is changed by another key-press. It is up to the micro processor to issue the read interrupt command to ascertain what caused the interrupt. If the micro processor does not issue the interrupt within a specific time, the old data is lost and only the latest data is reflected in the Interrupt Flag register.

In the standby mode of operation, only the hot-key will cause the interrupt flag to be set and the IRQ_N pin will be asserted. The micro processor should then read the interrupt to know what caused the wake-up operation before proceeding with the normal data communication or asserting STBY again if there is no action to be performed. Upon the first read of the hot-key data, the data in the buffer is cleared.

When the b4 of the above interrupt flag is set, then the µP should read the address 0x0F from the RTC register space to determine if the alarm was triggered. Only after determining this, the interrupt flag is cleared and the IRQ_N pin de-asserted.

The IRQ_N pin will only be de-asserted once the interrupt flags have been read. The chip will continue to send the interrupt periodically (approximately every 40us) to the main Host chip if the oscillator is down signifying to the Host chip that the frequency is out of spec.

7.4 Address setting command

This command sets an address of the display memory or the address of the RTC register map.

MSB							LSB
1	1	x	b4	b3	b2	b1	b0

The address range from 00h-0Fh represents the RTC register map. For writing data to RTC registers, initially the address command is sent followed by the RTC data.

10h-14h represents the 7-segment and discrete LED display correspondence. On power application, the address is set to 10h. In the auto-increment mode, when the address reached 0x14, the next ad-dress will be 0x10.

7.5 Display control and hotkey setting command

1	0	b5	b4	b3	b2	b1	b0

Bits b7-b6 = 10 is decoded as a display control and hotkey setting command. The subsequent bits are decoded as follows:

b5 = 0: sets display control for dimming setting as shown in the table below.

Display control and dimming setting when b5 = 0

b3.b0: sets dimming quantity.

0000: sets pulse width to 1/16.

0001: sets pulse width to 2/16.

0010: sets pulse width to 3/16.

0011: sets pulse width to 4/16.

0100: sets pulse width to 5/16.

0101: sets pulse width to 6/16.

0110: sets pulse width to 7/16.

0111: sets pulse width to 8/16.

1000: sets pulse width to 9/16.

1001: sets pulse width to 10/16 (default and recommended)

1010: sets pulse width to 11/16.

1011: sets pulse width to 12/16.

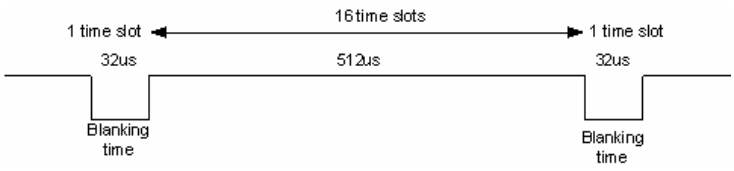
1100: sets pulse width to 13/16.

1101: sets pulse width to 14/16.

1110: sets pulse width to 15/16.

1111: sets pulse width to 16/16.

Figure 19. Blanking time



b4: Turns on/off display

0: Display off (keyscan continues)

1: Display on

When b5 = 1, the decoding is based on bits b1-b0 as illustrated below:

b1 b0 = 01: IR hot-key configuration of ADR and DATA. After this 3 bytes are sent which are in the form ADR+DATA to configure the hot-key for a particular device address. A maximum of 8 hot keys can be configured from a single device address or 4 hot-keys from two device addresses and so on. If more than 24 bytes in the form of ADR+DATA are sent, then the pointer moves back to the first ADR+DATA location.

b1 b0 = 10: FP hot-key configuration. Any of the 16 keys can be configured as hot-keys. 2 bytes of key data command are sent following this command to configure the front-panel hotkeys.

b4, b3 b2: Reserved

b1b0: 00 or 11 are treated as invalid commands and subsequent data bytes are ignored.

Remote control hot keys when b5 = 1

b1 b0: 01

Following 8-bit is sent to indicate the address for RC and subsequent 16-bit indicates the RC hot key value itself. So a total of 3 bytes are sent for one hot-key configuration. A total of 24 bytes are re-served for RC hot key configuration. Note that the customer code is programmable for the RC hotkey for both RCMM and R-STEP RC protocol.

Front Panel Hot Keys when b5 = 1

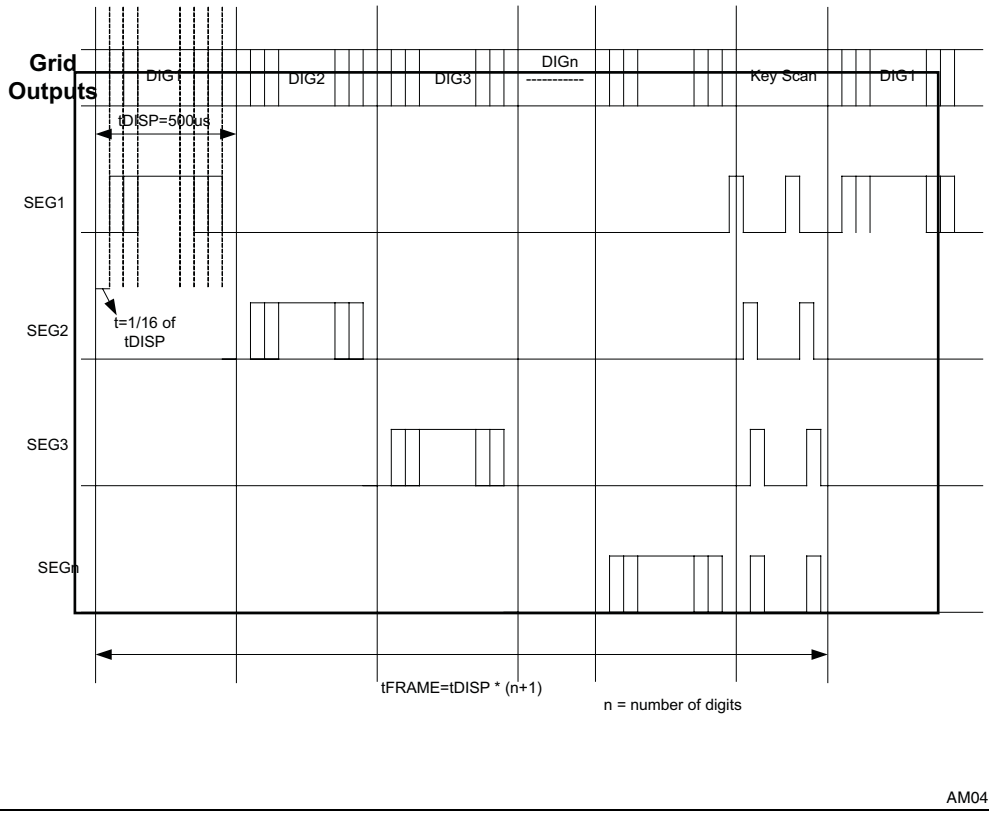
b1 b0: 10

Front panel hot keys can be configured by sending 2 bytes of key data to configure any key as hot-key from any of the 2 banks. Any number of keys can be configured as hot-keys.

When input key code matches any one of the predefined key codes stored in the internal RAM, the STLED325 de-asserts the STBY output.

7.6 Keyscanning and display timing

Figure 20. Keyscanning and display timing



The value is fixed by the internal clock from the oscillator.

One cycle of keyscanning consists of one frame, and data of 8x2 matrices are stored in the RAM.

Note that the keyscan is only at the end of the frame when the display is ON. When the display is OFF, the keyscan takes place continuously. The grid/digit is turned off during the keyscan.

8 State

8.1 Default state upon power-up

Table below shows the default state of the STLED325 upon power-up.

Table 30. Power-up defaults

Serial number	Function	Default state
1	Display	OFF
2	Key-scan	ON
3	IR	Disabled
4	Display mode	8 segment/1 digit
5	Display address	10H with address increment mode
6	RC protocol	Disabled
7	Dimming	10/16 duty factor
8	Hot keys (IR and FP)	Disabled
9	Guard timer	10s

8.2 Initial state

On power application, the 10/16-pulse width is set and the display shows the value configured in the LED display RAM before entering the standby mode. Thus if TUNE is required to be shown on the LED upon wake-up, then the user must write the corresponding digit and segments locations in the LED display memory before going into the standby mode of operation. The value of the display changes only after user configuration.

If the user wishes to display the RTC value during standby, then the user must configure the STLED325 by sending the appropriate command. If the user does not configure the STLED325 to display the RTC in standby, the LED shows the same value as was written previously in the LED display memory location.

Note that all the hot keys are disabled on power-up. Only the hot-keys (FP or RC) can be detected to wake-up the system from standby condition.

9 Remote control protocols

Contact STMicroelectronics for more information on RC protocols or refer to separate document (TBD).

10 Application information

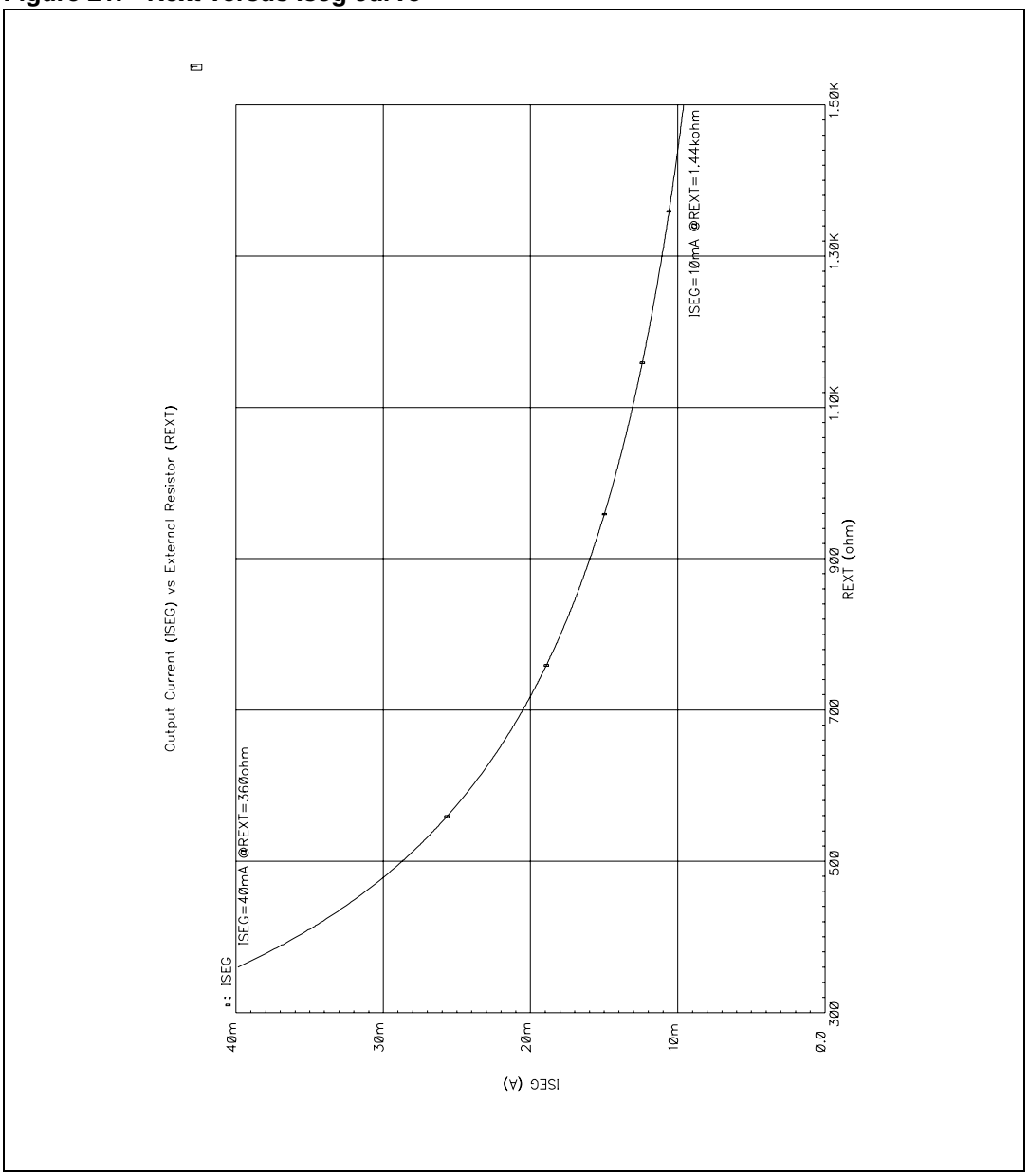
10.1 Power supply sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{CC} before applying any signals to the input/output or control pins.

10.2 I_{SET} variation with R_{SET}

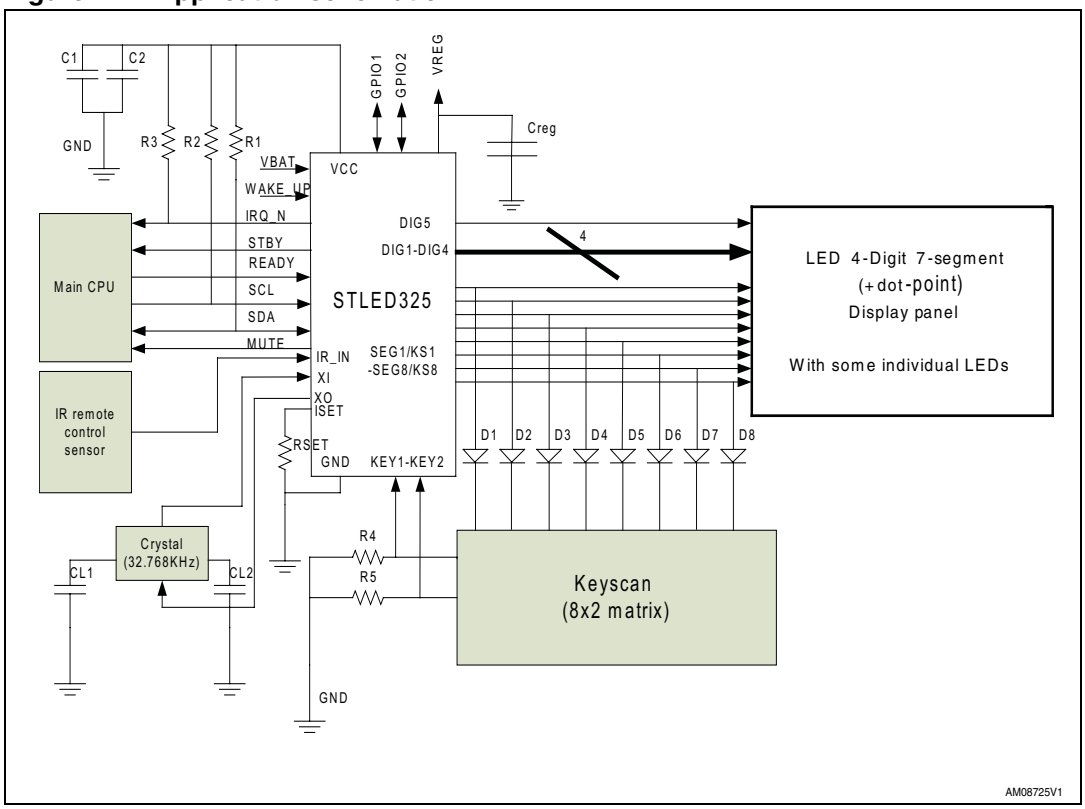
The graph of I_{SET} variation with R_{SET} is shown in *Figure 21*.

Figure 21. Rext versus Iseg curve



10.3 Application diagram

Figure 22. Application schematic



Resistors:

RSET = external resistor for current setting

R1 = 1-10 KO SDA external pull-up resistor

R2 = 1-10 KO SCL external pull-up resistor

R3 = 1-10 KO IRQ_N external pull-up resistor

R4-R5 = 10 KO external key-matrix pull-down resistors

Capacitors:

C1 = 33 µF (25 V) electrolytic

C2 = 0.01-0.1µF (25V) ceramic

Creg=0.1 uF

CL1 = CL2 = 25pF

Diodes

D1-D8 = 1N4148

Supply voltage

V_{CC} = 5 V ± 10%

11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 31. QFN32 (5 x 5 mm) mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	3.35	3.45	3.55
E	4.85	5.00	5.15
E2	3.35	3.45	3.55
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 23. QFN32 package dimensions

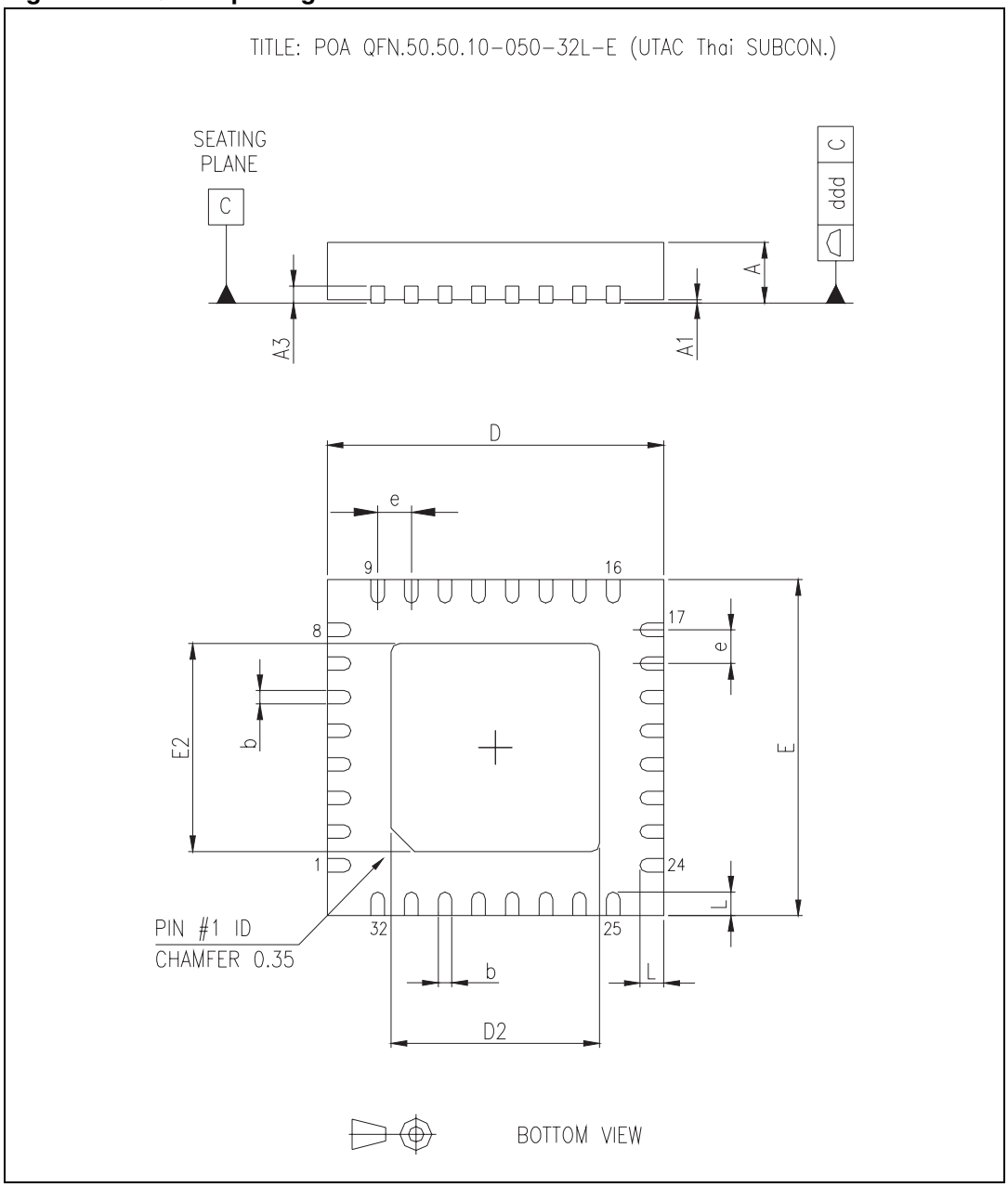
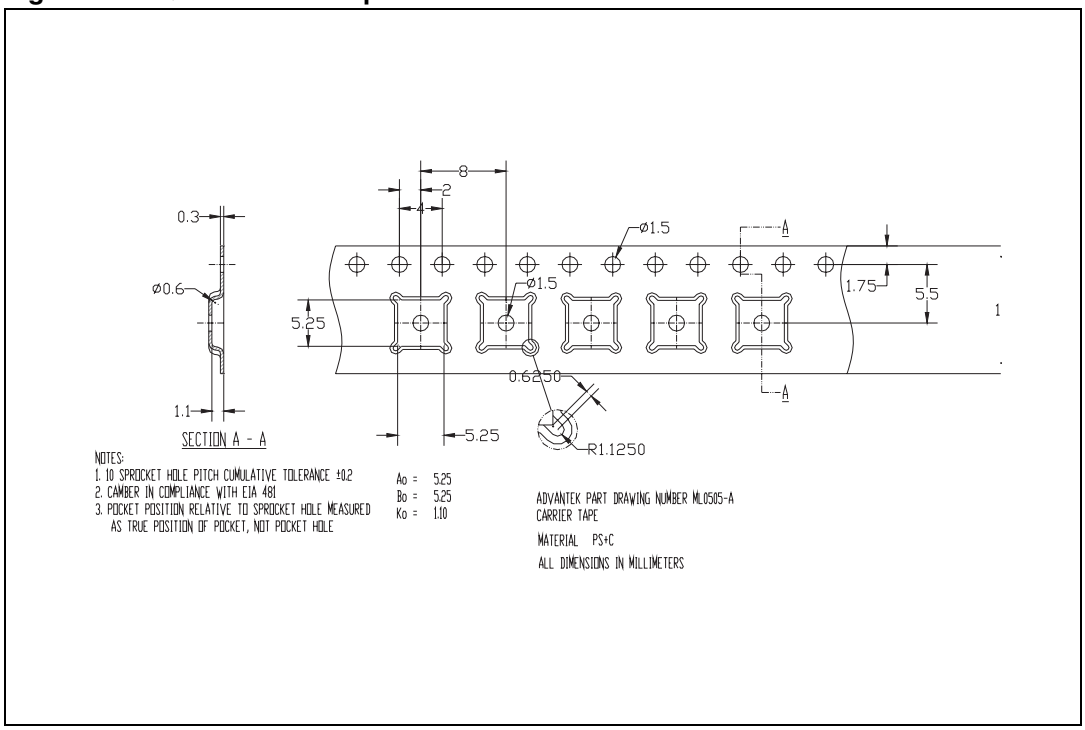


Figure 24. QFN32 carrier tape



12 Revision history

Table 32. Document revision history

Date	Revision	Changes
27-Apr-2011	1	Initial release.

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